A NEW APPROACH TO REDUCE THE CAPACITANCE VALUE IN A BINARY-WEIGHTED SWITCHED CAPACITOR DIGITAL-TO-ANALOG CONVERTER

A thesis submitted
in partial fulfillment of the requirements
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By
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Under the Supervision of
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to the

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INDIAN INSTITUTE OF TECHNOLOGY, KANPUR
APRIL –2002.

CERTIFICATE

This is to certify that the work contained in this thesis entitled **"A NEW APPROACH TO REDUCE THE CAPACITIVE VALUE IN A BINARY-WEIGHTED SWITCHED CAPACITOR DIGITAL-TO-ANALOG CONVERTER"** by Phalguni Bala has been carried out under my supervision and that this work has not been submitted elsewhere for the award of a degree.

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April 2002.

Abstract

Switched-capacitor digital-to-analog converter with binary-weighted capacitor array suffers from the disadvantage that the area required to fabricate the capacitors doubles with each additional bit of resolution. In this work, a modified architecture is proposed, which overcomes this disadvantage by using the same value of capacitor for each bit of the DAC. This is achieved by trading the frequency of operation for the area of the DAC. Simulated results for the proposed architecture for 0.5μm CMOS technology show INL and DNL less than 0.3LSB at a conversion frequency greater than 1MHz.

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It has been a real privilege to be a M. Tech student in the Electrical Engineering department at the Indian Institute of Technology, Kanpur. My experience here has been full of opportunities to learn from a faculty and student body with a wide and deep expertise in engineering. I would like to directly thank those people in the department who were particularly instrumental in contributing to my experience at IIT, Kanpur.

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Phalguni Bala
(Phalguni Bala)

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Chapter 1

Introduction

1.1 Introduction and Review of Available DAC Architectures

Signal from the real world signal is analog in nature. But most of the signals are processed in digital domain. The digital signal processor has developed rapidly due to integrated circuit technology over the past 25 years. There are several reasons why digital signal processing of an analog signal may be preferable to processing the signal directly in the analog domain. First, accuracy considerations play an important role in determining the form of the signal processor. Second, the digital signals are easily stored on magnetic media (tape or disk) without deterioration or loss of signal fidelity. As a consequence, the signals become transportable and can be processed off-line. The digital signal processing method also allows for the implementation of more sophisticated signal processing algorithms, which is difficult to perform precise mathematical operations on analog signal form. And, in some case, a digital implementation of the signal processing system is cheaper than its analog counterparts. The block diagram of a typical signal processing system is shown in the Figure 1.1. As the figure illustrates, the digital signal processor is in between processed and unprocessed analog signal domain. So two times conversion of the signal from analog to digital and digital to analog is needed. Conversions of signals are done with the help of two types of signal interpreters. Analog-to-digital converter converts

analog signal into equivalent digital signal and the digital-to-analog converter does exactly the opposite job. They are the backbone of a mixed signal system.

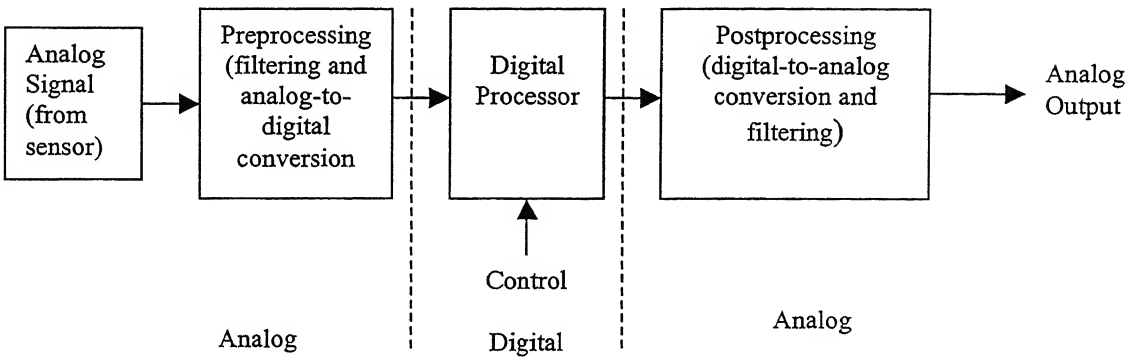


Figure 1.1: The Block Diagram of a Typical Signal Processing System

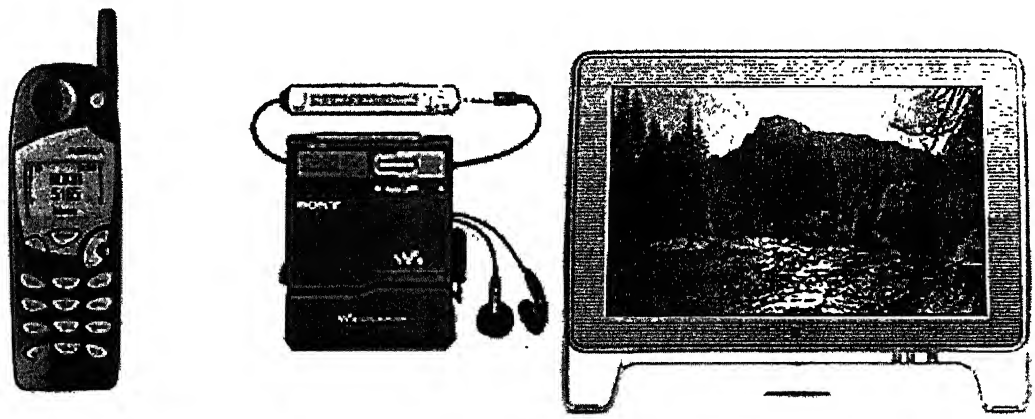


Figure 1.2: Digital devices from low frequency to high frequency. The Nokia cell phone, Sony mini disc player and flat panel display.

A few examples of digital systems where A/D and D/A converters are used, are illustrated in the Figure 1.2. The recent growth of mixed signal applications such as wireless communication and digital audio/video applications has fueled the design effort of the digital-to-analog converter (DAC). Various system requirements are pushing the researchers to invent new architectures of DAC. Moreover, these systems are tending to be mobile, giving rise to new different system specifications. Most critical aspects of the design of a mobile device are low power and minimum area and full integration of analog

and digital circuits. The mobile systems are battery operated so that power dissipation in a chip directly affects the lifetime of the battery. On the other hand if a circuit supports full integration with the present day digital VLSI circuit and if it takes smaller area, then many functions can be done with a single chip. Full integration makes a device cost effective, which is the ultimate goal of a designer. Now a day most of the digital VLSI circuits are fabricated in CMOS technology, so any circuit designed should be fabrication friendly to CMOS technology.

Many DAC topologies are available, like resistor-string, current-scaling, charge-scaling, pipelining, cyclic architecture and combinations of them [1]. Each topology has various strengths and weaknesses, which can be summarized by several criteria: integral non-linearity (INL), differential non-linearity (DNL), monotonicity, chip area, matching accuracy of different components, conversion frequency and of course full integration. The binary-weighted resistor string is one of the simplest architecture of a DAC. It is an array of resistors and switches. The resistor array acts as voltage divider network. For a particular input combination only one node is selected [3]. The node voltage is proportional to magnitude of input digital word. Though it has the simplest circuit architecture, resistor string DACs have fallen out of interest due to several reasons. The number of resistor elements that required for an N bit DAC is 2^N. With the exponential growth in the number of elements clearly higher order bit requirements size of the DAC grows prohibitively large. Additionally continuous flow of current through the resistors dissipates a large amount of power [3]. Furthermore, the absolute resistor values in CMOS fabrication process varies by great amount from slow to fast processes, which can create significant differences in power consumption from chip to chip. Finally, resistor-ladder DACs tend to be slow due to the large resistance load on the output. This can be avoided in several ways (small resistor values or large output buffers), but each method burns a significant amount of power. Thus, in modern CMOS processes, a resistor-ladder DAC is probably not the best solution.

A popular DAC architecture is current steering DAC [3]. Binary-weighted version of an N bit DAC has N number of current source ranges from I to 2^{N-1}I. And thermometer coded [see Appendix A.] version has $2^N - 1$ number of current sources having identical value I. The magnitude output current is linearly related to the magnitude of input digital

code word [3]. With a trans-resistance amplifier the output current can be transformed into equivalent voltage [1][4]. The unit-element arrays have the drawback of much larger area because of extra binary to thermometer code converter, but they have the benefit of guaranteed monotonicity. Binary arrays contain no such guarantee. During midcode transitions where the MSB source is varying one direction and the LSB sources are varying another direction (for 3 bit DAC, binary 011 to 100 transition corresponding to a decimal 3 to 4 transition), the output can change by substantially more than 1 LSB – causing a potentially substantial deviation from the ideal value of the output of binary weighted current steering DAC. But in unit-element current steering DAC, the analog output is varied by one switch turning on or off. Thus a binary array is not a good choice for applications when monotonicity is an important criterion.

A second benefit of thermometer coding is that glitches do not contribute to non-linearity. The size of the glitch in thermometer-coded DACs is proportional to the number of switches at a given sample time. When the step is small (i.e. one LSB changes), the glitch is small, and when the step is larger, the glitch is larger. However, since the number of switches that change is proportional to the size of the signal step, the magnitude of the glitch is directly proportional to the magnitude of the signal step. Thus the glitch does not cause any non-linearity in the converter's analog signal.

A third advantage of unit-element DACs over binary-weighted types is matching requirement of the current sources. The matching requirement is significantly reduced, as 50% matching of the unit current source results in a DNL of under 0.5 LSB. For the binary-weighted version, the order of the matching of the current sources is determined by the weight of the bit. The matching of the MSB current source transistor must be extremely accurate [3]. DNL is the limiting factor for the binary weighted digital-to-analog converter and where as INL is the limiting factor for thermometer coded counterpart.

The advantage of both types of current steering DACs is high current driving capability inherently in the system. Since no buffer is necessary to drive resistive loads, these DACs typically are used in high-speed applications [3]. Both the DACs have common problems, they consume large amount of active area of the chip and it also dissipates a large amount of power. These make the DACs unattractive, where area and power constraints are there.

Switched capacitor (SC) DAC is another important family of DACs [10]. The advantage of all SC DACs is it can be easily fabricated with any other digital VLSI circuit on the same chip. Because most of the digital VLSI circuits are fabricated in CMOS technology and in CMOS technology good quality leakage free capacitor, which is the heart of SC circuit, can be fabricated with high degree of precision. The simplest DAC architecture among all other SC DACs is binary-weighted charge-scaling DAC. The circuit is similar to the binary-weighted current scaling DAC, with the difference that in place of binary-weighted current source binary-weighted capacitors are used there. Basically, the output from a SC DAC is charge, where magnitude of charge is proportional to the magnitude input digital word. While this charge is stored in a capacitor, causing proportional voltage across the capacitors [1][3]. The binary-weighted SC DACs also suffer from higher DNL problem.

The capacitor associated with the MSB of an N bit binary weighted SC DAC is 2^{N-1} C, which grows exponentially with addition of each new bit to the input digital word. The consequence is that it takes large amount of die area to fabricate the capacitors and binary-weighted DAC architecture becomes unattractive for high-resolution applications. Reducing the capacitor value could be one of the solutions to the problem, but parasitic capacitance and signal-to-noise requirement set the lower limit of the capacitor value [1][2]. The other method proposed [4] to reduce the capacitor area is to use two stages of capacitor blocks with an additional charge attenuating capacitor [for detail discussion see Charter 2]. But still due to exponential dependency of the maximum capacitor value it takes a large amount of space to fabricate the capacitors. So beyond 8-9 bits resolution this type of DACs are not suitable. The binary-weighted SC DACs also suffer from higher DNL problem.

The other main two types of switched capacitor DACs are cyclic DAC [11] and pipeline DAC [1][2]. Both of these DACs use pseudo-"sample-data" approach. Implementation of these architectures using switched-capacitor is relatively easy [3] and hence suitable for fully integrated circuits. Cyclic DAC, also called sequential DAC converts one bit of digital word in one clock pulse. So it uses N number of clock cycles to convert a digital word of N bits length. This architecture is very popular in slow speed application because of its simplicity of operation. Accuracy of cyclic DAC depends on the

gain of the amplifier, adder and sample and hold (S/H) circuit [11][2]. Speed of operation can be increased with the modified architecture called pipeline DAC. Pipeline DAC is cascaded architecture of N number of cyclic DAC [1][3]. Pipeline DAC converts digital input in one clock pulse but it needs N clock cycles to get analog output for one combination of digital word. That means the latency of the pipeline DAC is N clock cycles. It is used for very high-speed operation. Like cyclic DAC, the precision of this type DAC depends on the accuracy of the gain of the amplifiers used, accuracy of the adders and S/H circuits [3].

There are other possible architectures obtained by combining of the different architectures discussed above. The combination is to be chosen such that the new architecture has the advantages of both parent architectures [1] and will satisfy the system requirements, which is not possible with one particular architecture.

This thesis presents a new architecture of the SC DAC (which does the equivalent operation of a binary-weighted SC DAC) which has the same value of capacitor for every bit. That makes the active area very small compared with any other binary weighted counterpart. Instead of varying the capacitor, the switching frequency is varied depending on the weight of the bit. In this manner the speed is traded off with the area of the circuit.

1.2 Thesis Organization

Following this chapter, Chapter 2 describes the operation and performance of different types of switched capacitor DAC architectures. At the end of the chapter the architecture of the new DAC designed in this work is discussed in detail.

Chapter 3 describes the different design aspects, like matching, sizing of analog switches, power consumption, speed of operation, signal-to-noise ratio, bandwidth requirement etc.

In Chapter 4 the results obtained by simulating the extracted circuit are provided.

Conclusions and future scope of work are presented in the Chapter 5.

Chapter 2

Switched Capacitor Digital-to-Analog Converter Architectures

2.1 Introduction

The advent of analog sampled data technique and CMOS technology has made the design of a digital-to-analog converter a viable approach. Switched capacitor circuits are more suitable for combining analog and digital functional blocks in CMOS technology. Primary reason for this is that digital VLSI circuits are typically implemented in CMOS technology. On the other hand, the CMOS technology is able to provide good quality capacitor with 0.1% accuracy (even better with careful fabrication) good quality switch and op-amp, which are the main elements of a SC circuit. Additionally, frequency response of the fabricated capacitor in CMOS technology is also very good.

So switched-capacitor digital-to-analog converters are preferred over other DAC architectures. Besides this, a SC implementation also has advantage over current mode counterpart in reduced clock jitter sensitivity and data dependent glitches that can cause distortion. SC DACs can be built using several different topologies. Each architecture has various advantages and disadvantages, which can be expressed by several criteria: integral non-linearity (INL), differential non-linearity (DNL), monotonicity, die area, matching of different components and conversion frequency.

This chapter briefly examines the different architectures and discusses their pros and cons in Section 2.2. It also goes through detail discussion about the new architecture in Section 2.3.

2.2 Switched Capacitor DACs

Popular SC DAC architectures are binary weighted capacitor, two-stage binary weighted capacitor DAC, SC cyclic and pipelining DAC.

2.2.1 Binary Weighted Switched Capacitor DAC with Stray-insensitive Switching Scheme

The simplest DAC architecture among all other SC DACs is binary-weighted SC DAC [Figure2.2.1][1][3][4][10]. This has an array of capacitors, having binary-weighted values. The capacitor associated with the LSB of the digital code has the minimum value C. The capacitor associated with the next higher order bits have the values 2C, 4C and so on up to $2^{N-1}C$ for MSB capacitor. The bottom plates of the capacitors switch between V_{REF} and ground depending on the corresponding bit status. If the LSB capacitor switches once, it transfers $Q_0=CV_{REF}$ amount of charge to charge integrating capacitor C_{int}. Similarly in one switching cycle the capacitor associated with i^{th} bit transfers $Q_i=2^iC$ (i= 0 to N-1) amount of charge to the capacitor C_{int}. Figure 2.2.1.2 illustrates the timing sequence of different signals of the circuit. For proper circuit operation a non-overlapping two-phase clock (ϕ_1,ϕ_2) is required. The circuit operates in two stages. In stage one (ϕ_2 is high), C_{int} is discharged through RESET switch and all other capacitors are charged to V_{REF} (reset & pre-charge phase). Next, in stage two (ϕ_1 is high), RESET switch turns off, and the bottom plate of the capacitors associated with the bits having binary value '1' switch to ground at the rising edge of the clock ϕ_1(charge transfer phase). This causes the transfer of charge from the binary-weighted capacitor to the charge integrating capacitor C_{int}. So amount of charge transfer and hence voltage across the capacitor C_{int} is proportional to the magnitude of input digital word.

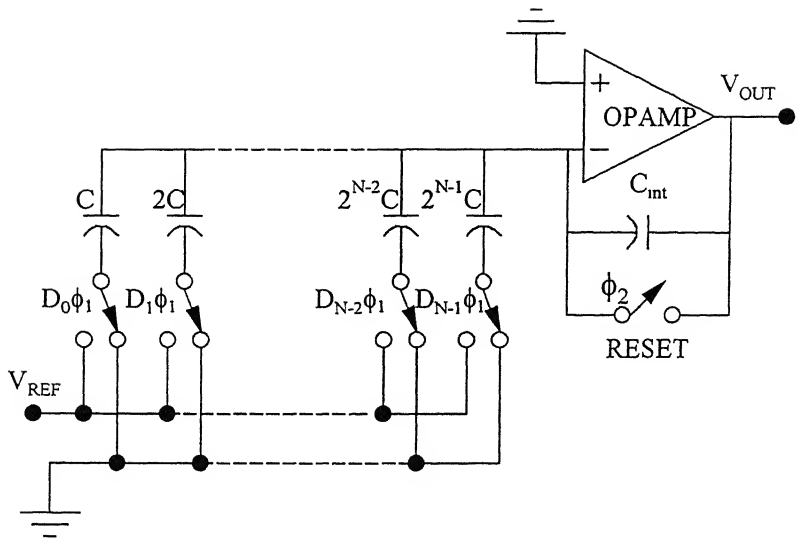


Figure 2.2.1.1 Binary Weighted SC DAC

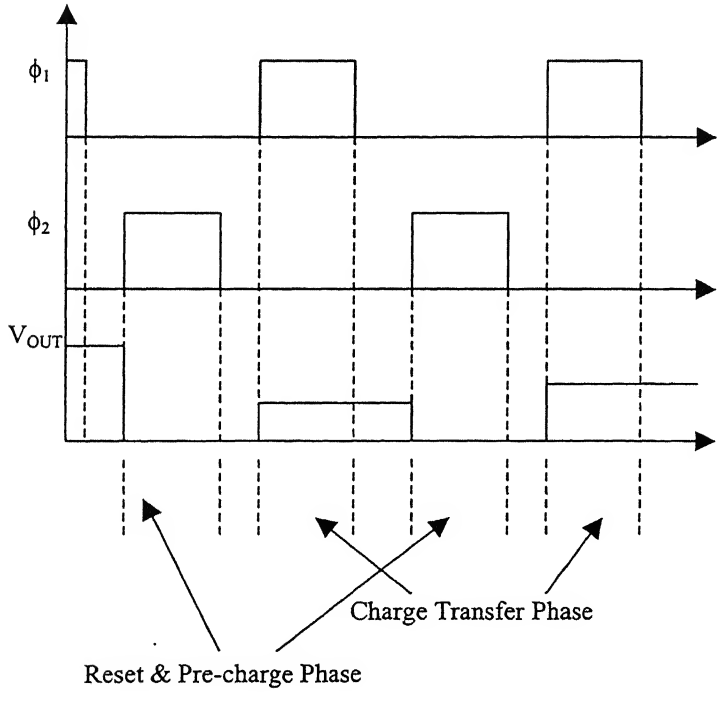


Figure 2.2.1.2: Timing diagram of Binary Weighted SC DAC.

Then the output voltage can be written as,

$$V_{out} = \frac{C}{C_{\text{int}}} V_{REF}\left[2^{N-1} b_{N-1} + \ldots + 2b_1 + b_0\right] \quad \text{.....(Eqn 2.2.1.1)}$$

Where b_i's are either '1' or '0'.

In every clock cycle the output is updated with new value of analog signal proportional to the digital code.

The major problem with the DAC is if capacitor values differ from the ideal value the output voltage no longer remain proportional to the magnitude of the digital code, giving rise to non-zero value of INL and DNL.

Let us examine the INL and DNL due to mismatch in capacitor value of a binary-weighted SC DAC, which limits the resolution of the DAC. Let us consider capacitor associated with k^{th} bit of the digital input deviates ΔC_k amount from the ideal value, then the capacitance of the k^{th} capacitor is

$$C_k = 2^{k-1}C + \Delta C_k \quad for\ k = 0,1,2....N-1 \quad .....(Eqn.2.2.1.2a)$$

And with another assumption, capacitor corresponding to MSB has maximum positive mismatch error and remainder of the bits contains a maximum negative mismatch error, that is

$$\sum_{k=0}^{N-1} \Delta C_k = 0 \quad .....(Eqn.\ 2.2.1.2b)$$

So the worst case INL becomes of the form given below [see. Appendix B]

$$|INL|_{\max} = \frac{2^{N-1}C + |\Delta C|_{\max,INL} - 2^{N-1}.C}{C_{\text{int}}}.V_{REF} = \frac{|\Delta C|_{\max,INL}}{C_{\text{int}}}V_{REF} \quad .....(Eqn.\ 2.2.1.3)$$

Similarly, the worst case DNL can be written as [see. Appendix B]

$$DNL_{\max} = \frac{\left[2^{N-1}C + |\Delta C|_{\max,DNL} - \left(\sum_{k=0}^{N-2} 2^k C - |\Delta C|_{\max,DNL}\right)\right] - C}{C_{\text{int}}}V_{REF} = \frac{2|\Delta C|_{\max,DNL}}{C_{\text{int}}}V_{REF}$$

$$.....(Eqn.\ 2.2.1.4)$$

From the equations Eqn.2.2.1.4. and Eqn.2.2.1.5 it is clear that the DNL requirement is more stringent in binary weighted DAC than the INL requirement. Thus DNL requirement sets the resolution of the DAC. The maximum value of DNL should be less than ½ LSB. This gives upper bound of capacitor mismatch as

$$2.\frac{|\Delta C|_{\max,DNL}}{C_{\text{int}}}V_{REF} \le \frac{1}{2}\frac{C}{C_{\text{int}}}V_{REF} \quad \Rightarrow \quad \frac{|\Delta C|_{\max,DNl}}{C} \le \frac{1}{4} \qquad \text{.....(Eqn. 2.2.1.5)}$$

The main limiting factor of a binary weighted capacitor DAC is that it takes large amount of chip area, because the capacitor associated with the MSB of an N bit DAC is $2^{N-1}C$, which doubles with addition of a bit to the digital word. The parasitic capacitance and signal-to-noise requirement set the minimum value of capacitor C. So beyond 8-9 bit resolution this type of DAC is hardly used.

2.2.2 Two-stage Binary Weighted Switched-Capacitor DAC

Yee, Terman and Heller proposed another architecture [4], which relaxes the large area requirement of the binary-weighted SC DAC, discussed in the previous section. The schematic of an eight-bit DAC is shown in the Figure 2.2.2.1. It has two blocks of array of binary-weighted capacitors. One block is for four LSBs and other block is for four MSBs. The capacitor C_{attn} acts as charge attenuator to the LSB capacitor block. The operation and timing diagram of the DAC is very much similar to that of binary-weighted SC DAC. When ϕ_2 is high all the binary weighted capacitors charge to reference voltage V_{REF} and the capacitor C_{int} discharges. In the next phase the capacitors switch to ground node and transfers charge to C_{int}. If LSB is '1' the capacitor associated with LSB transfers $C/16V_{REF}$ amount of charge to the capacitor C_{int}. Similarly, the capacitor associated with next higher order bits transfer 2-times, 4-times and so on of $C/16V_{REF}$ charge to C_{int} provided the corresponding bits are '1'. Then the output voltage can be written as

$$V_{out} = \frac{C}{16C_{\text{int}}} V_{REF}\left[2^{N-1} b_{N-1} + \ldots + 2b_1 + b_0\right] \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (Eqn\ 2.2.1.2)$$

Eqn2.2.1.2 shows that the output voltage again becomes proportional to the input digital code.

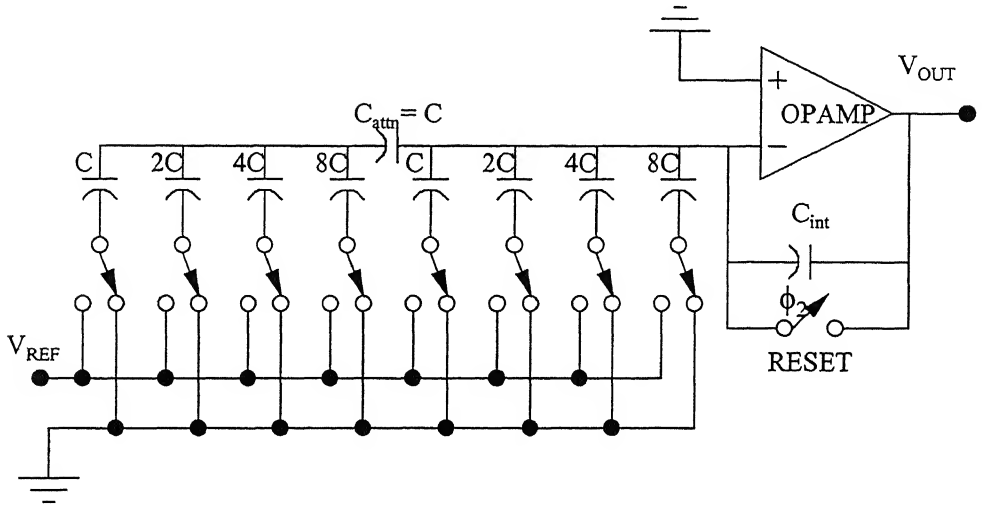


Figure 2.2.2.1: Two-stage Binary Weighted Switched-capacitor DAC.

Two-stage binary-weighted SC DAC has all other limitation similar to the binary-weighted SC DAC. The DNL of the DAC due to capacitor mismatch limits the resolution of the DAC. This DAC also suffers from same monotonicity problem as the binary-weighted version does. But the major advantage of two-stage N-bit DAC is the maximum capacitor value is $2^{N/2}C$, which is very good improvement in terms of area saving requirement [4]. Still it takes a large amount area because of exponential dependency of the maximum capacitor value with the number of bits of the input digital word.

2.2.3 Cyclic SC DAC

Cyclic DAC also called serial DAC is a very popular DAC architecture. It operates in discrete time domain mode. So implementation of the DAC with switched capacitor circuits is much easier. The algorithm of a cyclic DACs is illustrated in the Figure 2.2.3.1[1][3]. The operation of the DAC is very simple. It has a digital parallel-to-serial converter, adder, S/H circuit, amplifier and switches. It converts one bit in each clock pulse. The operation as follows: initially the S/H circuit is reset, then adder input 'A' is connected to either V_{REF} or ground in every clock pulse depending on the status of a certain bit. The operation starts with D_0 and ends with D_{N-1}. The adder adds V_{REF} or ground to the feedback signal depending on the input bit status. The feedback voltage plus either V_{REF} or zero voltage is sampled and held by S/H circuit in every clock pulse for the next clock pulse. Amplifier with a gain of ½ feeds the feedback signal to the adder. The output voltage at end of i^{th} clock pulse can be written as

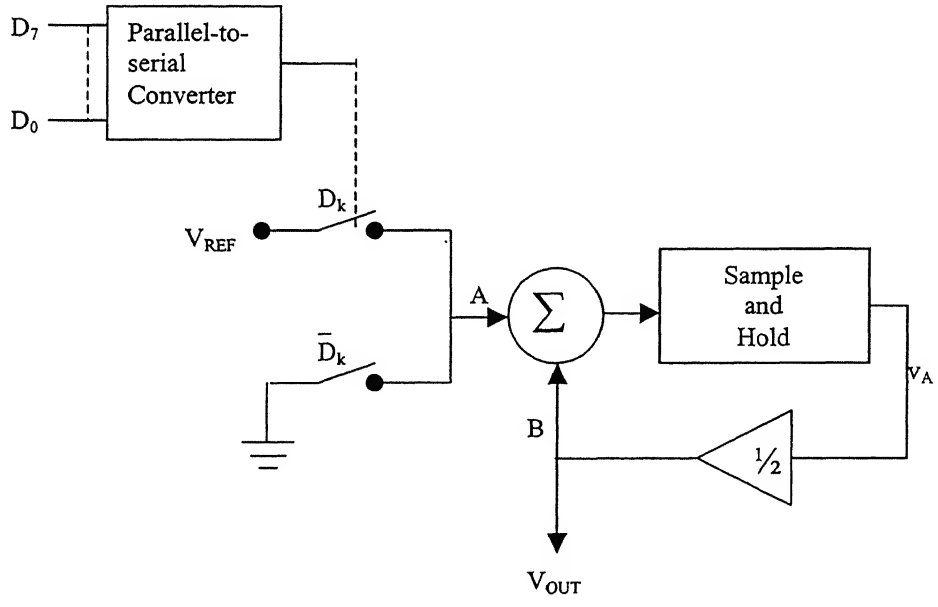


Figure 2.2.3.1: Schematic of Cyclic DAC

$$V_{OUT} = \left(b_{i-1}.V_{REF} + \frac{1}{2}.v_A(i-1) \right).\frac{1}{2} \quad \text{.....(Eqn. 2.2.3.1)}$$

From the Eqn. 2.2.3.1 it is clear that final output voltage is proportional to the magnitude of digital input. Cyclic DAC takes N-clock cycles to convert an N-bit digital input. The output analog signal is updated after every N-clock cycles. So the latency of the DAC is N clock cycles. It is generally used in slow speed operation. Though the operation of the DAC is quite simple the maximum achievable resolution of the DAC depends on several factors. The gain of the amplifier needs to be highly accurate, which is limited by the accuracy of the passive element such as capacitor. Similarly the adder, sample-and-hold also need to be N-bit accurate. The DAC has an additional feature it is inherently monotonic. So this DAC can be used where monotonicity is an important criterion.

2.2.4 Pipeline DAC

As discussed in the very previous section, the cyclic DAC needs N-clock cycles to convert a particular digital input of N-bit length. Longer conversion cycle makes the cyclic DAC unattractive in high-speed applications. Conversion can be done in one clock cycle with the modified architecture shown in the Figure 2.2.4.1 [1][2]. It has N number of pipelined stages. All the stages are similar to the cyclic DAC. Only difference is that adder input B (Figure 2.2.3) is connected to the output of the previous stage. The sequence of operation is similar to that of the cyclic DAC. To convert a certain digital input the DAC takes N-clock pulses. But due to pipelined conversion process, the conversion of N digital words goes on at a time and the output of the DAC is updated with new value in every clock pulse [1][2]. So effectively the conversion is done in one clock cycle. But the latency of the DAC remains same as that of cyclic DAC.

The disadvantage of the DAC is clear from the schematic of the DAC. It needs N times more hardware that of a cyclic DAC. Since effective conversion time is only one clock pulse, it is suitable for high-speed operation, where area constrains is not so critical. The resolution of the DAC depends on the accuracy of gain of the op-amp, S/H circuit and adder. Like cyclic DAC pipeline DAC is inherently monotonic.

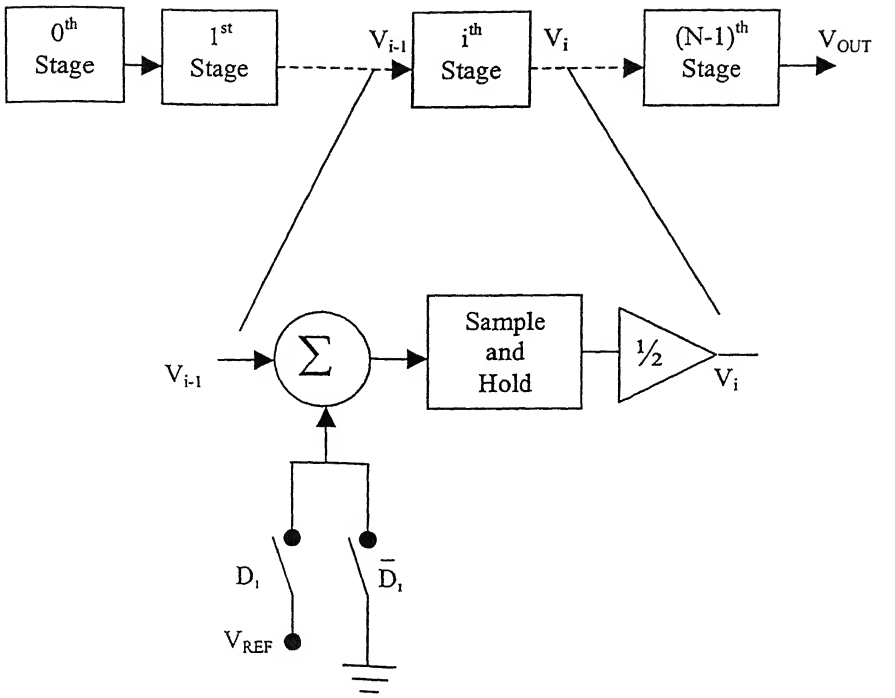


Figure 2.2.4.1: N-stage Pipeline DAC.

2.3 The New Architecture of Switched-Capacitor DAC

Binary-weighted SC DAC and its variant two-stage binary-weighted SC DAC, discussed in the section 2.2.1 and 2.2.2, take a large amount of area to fabricate the capacitors. As the resolution of the DAC increases the area requirement of the DAC increases rapidly. This limitation makes it difficult to implement the DAC beyond 8-9-bit resolution in a cost-effective manner. The capacitor associated with i^{th} bit of the input digital word transfers 2^iCV_{REF} amount of charge to the charge integrating capacitor C_{int} in one conversion cycle [see Section 2.2.1]. Suppose the capacitor associated with each bit is made the same. In that case a charge of 2^iCV_{REF} will have to be supplied. The different ways in which this could be done are as follows:

Option 1: Instead of varying the capacitor value the reference voltage can be varied. The schematic of the DAC with binary-weighted reference voltages is shown in the Figure 2.3.1. In one switching cycle the capacitor associated with LSB transfers $C \times V_{REF}$ amount of charge to charge-integrating capacitor C_{int}. Similarly, next higher significant

bits transfer $C\times2V_{REF}$, $C\times4V_{REF}$ .... $C\times2^{N-1}V_{REF}$ amount of charge to the capacitor C_{int}. So the charge transferred by i^{th} bit can be written as $C\times2^{i}V_{REF}$, where i= 0 to N-1. This is exactly same as that of binary-weighted SC DAC. As said earlier that the DAC needs N number of reference voltage sources having binary-weighted values. The accuracy of the DAC depends on the accuracy of all the reference voltages, provided all the capacitors are matched. It is not so easy to design voltage sources with very accurate values covering the range V_{REF} to $2^{i}V_{REF}$ and the voltage sources also take a large amount of space on the die. The area saved by reducing the capacitor value is somewhat nullified by the N number of reference voltage sources. So this type of architecture does not provide a better solution to the problems of a binary-weighted SC DAC.

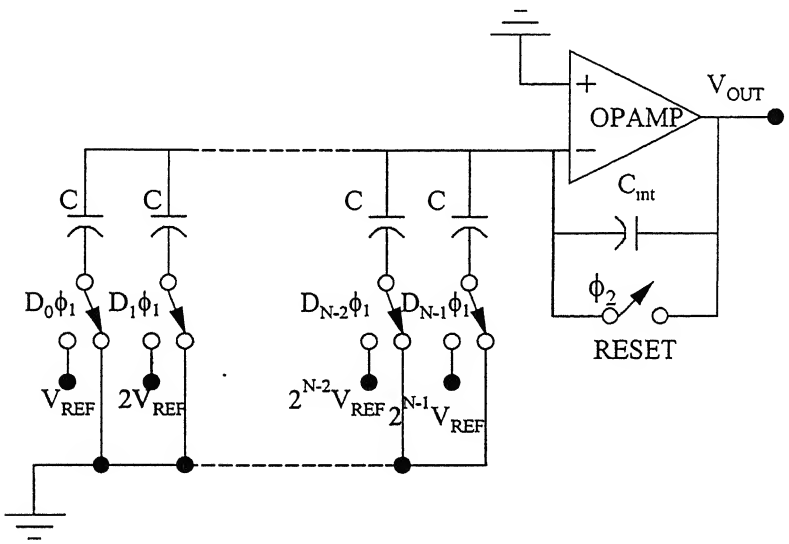


Figure 2.3.1: New DAC architecture with varying reference voltage.

Option 2: Another possibility, where the reference voltages for all the bits are kept the same, is the number switching cycle of a capacitor associated with each bit is varied in during the conversion period $T_S=1/f_S$ binary weighted fashion. The architecture is shown in the Figure 2.3.2a.

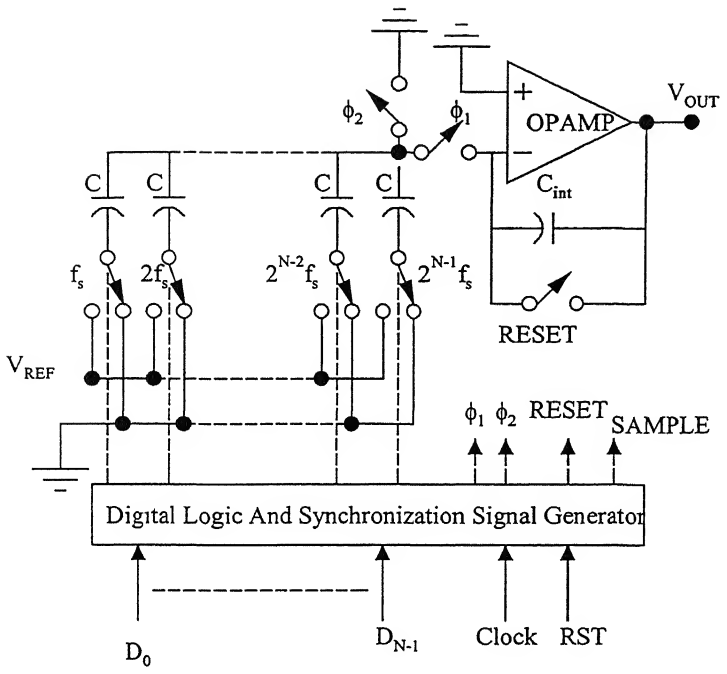


Figure 2.3.2a: New architecture of SC DAC with binary-weighted switching frequency.

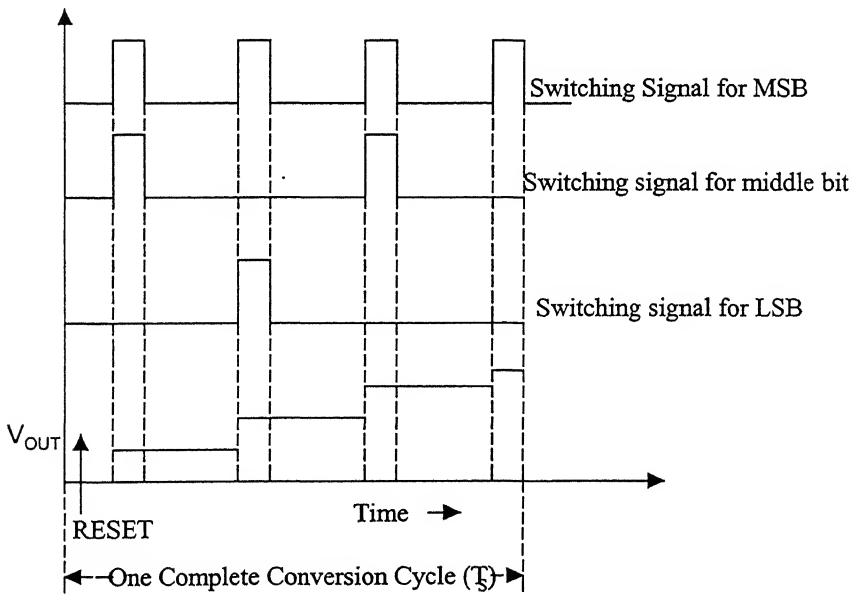


Figure 2.3.2b: Timing diagram of a 3-bit DAC with binary-weighted switching frequency

The operation of the DAC can be understood using timing diagram shown above. The capacitor associated with the bits starting from LSB to MSB switch once, twice, 4-times and so on up to 2^{N-1}times respectively over a period of time T_S. The timing diagram for a 3 bit DAC is drawn in the Figure 2.3.2b. The diagram shows that the capacitor associated with LSB, middle bit and MSB transfer charge once, twice and 4-times respectively over the time period T_S. The capacitors transfer CV_{REF}, $CV_{REF}\times 2$ and $CV_{REF}\times 4$ amount of charge to the capacitor C_{int}. Similarly for N-bit DAC the capacitors transfer CV_{REF}, $CV_{REF}\times 2$ ....$CV_{REF}\times 2^{N-1}$amount of charge over the conversion cycle T_S. Effectively the net charge transfer over T_S becomes exactly equal to that of the binary-weighted DAC.

If the charge transferred by each capacitor is averaged over the complete conversion cycle, then the switched-capacitor can be thought of as current sources having average value (from LSB to MSB) CV_{REF}/Ts, $2CV_{REF}/T_S$, $4CV_{REF}/T_S$ and so on.

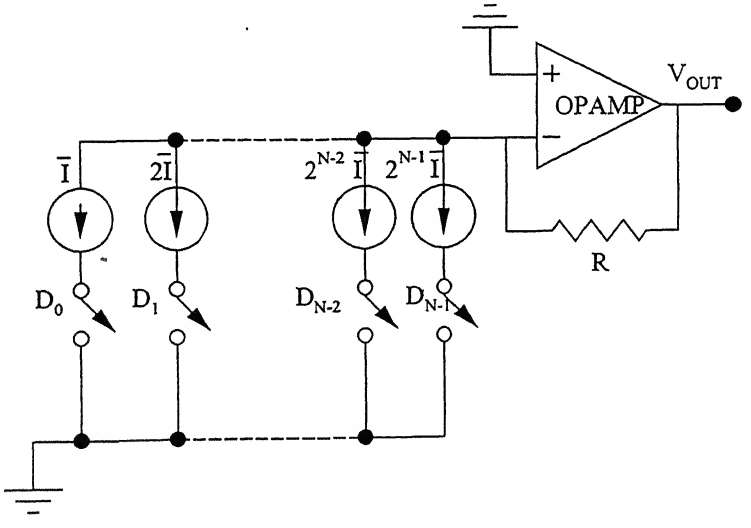


Figure 2.3.3: A current scaling DAC

So from this point of view, the proposed DAC can be seen as a kind of current scaling DAC [Figure 2.3.3] with average current associated with i^{th} is

$$\bar{I}_i = 2^i CV_{REF} f_S = 2^i \bar{I} \quad and \quad R = 1/C_{int}, \quad where, i = 0 \; to \; N-1.$$

The major problem with the proposed architecture is that it needs clock frequency of $2^{N-1}f_S$. For proper operation the op-amp that used to integrate charge should have unity gain frequency ~10times the maximum clock frequency. The finite unity gain frequency of the op-amp of the charge-integrating circuit limits the resolution and conversion rate of the DAC.

Option 3: The problem faced with binary-weighted switching frequency scheme can be reduced with the modified architecture. The modified architecture is combination of binary-weighted architecture and the binary-weighted switching frequency architecture. The circuit schematic is drawn in the Figure 2.3.2a. If the capacitor associated with MSB has the value 2C instead of C, then number of switching required to transfer $2^{N-1}CV_{REF}$ amount of charge is 2^{N-2} [Figure 2.3.4].

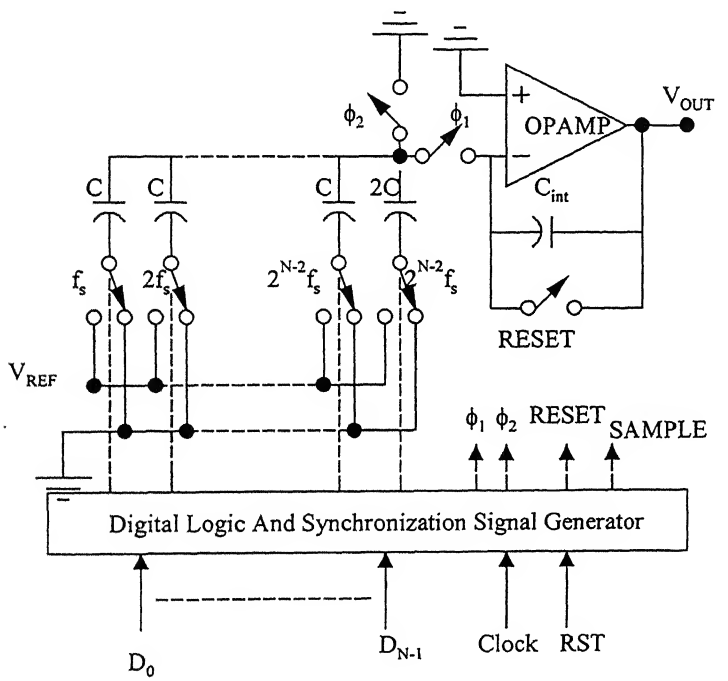


Figure2.3.4: SC DAC with binary-weighted switching frequency and 2C MSB capacitance

So the clock frequency becomes half of that required for the pure binary-weighted switching frequency architecture of Figure2.3.2a. In similar manner if the capacitor MSB and very next bit have the values 4C and 2C then the maximum number of switching required is 2^{N-3} over a period of time T_S. And the clock frequency further gets reduced. So this shows a way to trade off between capacitor area and speed of operation.

Option 4: Instead of a flat array of capacitance having same capacitance value C, if two-stage array of same value capacitance with a charge attenuating capacitor (as done in two-stage binary weighted SC DAC) is used then a tremendous amount speed improvement can be achieved. This will cost only an attenuating capacitor. Let us study the architecture of an eight-bit DAC. Figure 2.3.5 illustrates the complete circuit schematic of the DAC. It has two blocks of capacitor array. One block is for four lower significant bits of the input digital code and the other block is for other four higher significant bits. In between the blocks a charge attenuating capacitor C_{int} is connected. C_{int} attenuates the charge transferred from the lower significant-bit block. If any capacitor of LSB block switches once it transfers $CV_{REF}/16$ amount of charge to the capacitor C_{int}, causing $CV_{REF}/16C_{int}$ voltage across the capacitor. Now if the capacitors of the LSB block have the switching frequency f_S, $2f_S$, $4f_S$ and $4f_S$ then the average charge transferred over the period $T_S=1/f_S$ are $CV_{REF}f_S/16$, $2CV_{REF}f_S/16$, $4CV_{REF}f_S/16$ and $8CV_{REF}f_S/16$. Similarly the any capacitor of the MSB block transfers CV_{REF} amount of charge in one switching. And if capacitors of the MSB block have the same set of switching frequency, then the average charge transferred over the same period T_S are $CV_{REF}f_S$, $2CV_{REF}f_S$, $4CV_{REF}f_S$ and $8CV_{REF}f_S$. Hence the average charge transferred by the capacitors from LSB to MSB have binary-weighted relation, similar to the two-stage binary-weighted capacitor SC DAC.

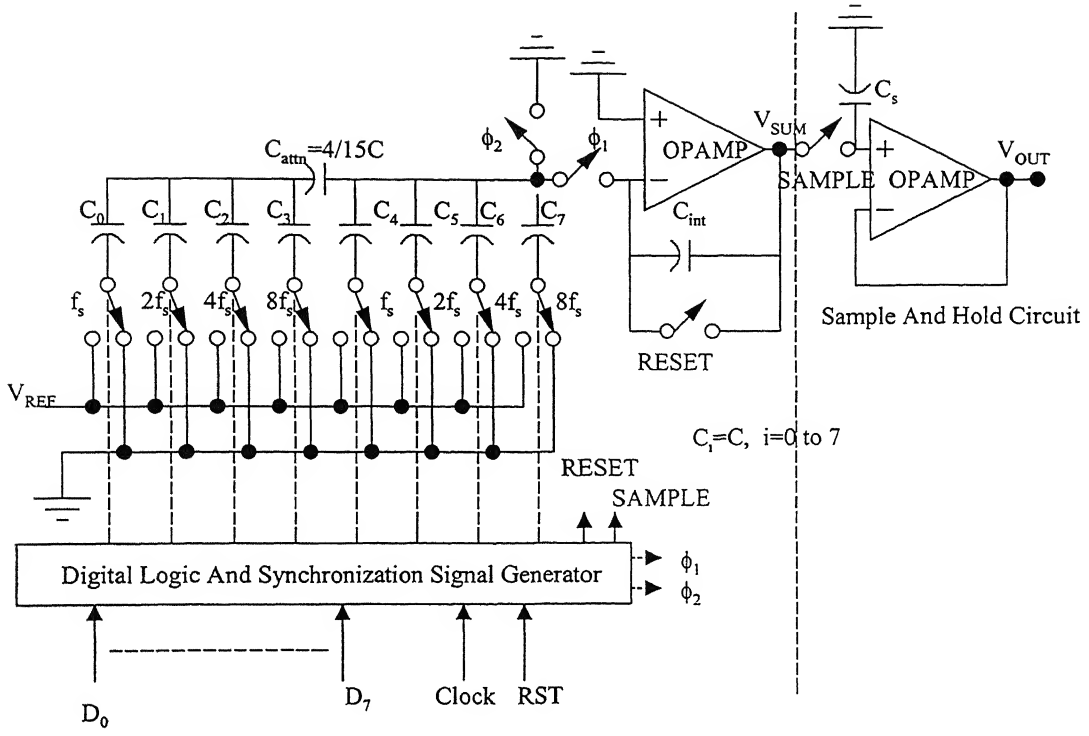


Figure 2.3.5a: Two-stage binary-weighted switching frequency DAC.

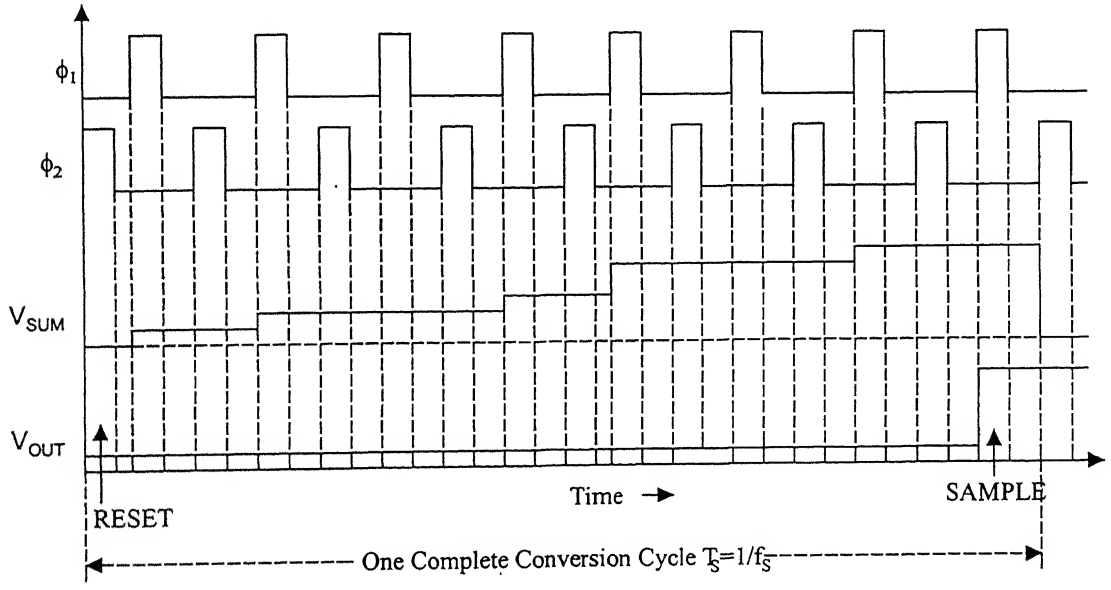


Figure 2.3.5b: Typical voltage waveforms at different nodes of the new SC DAC

The timing diagram shows typical voltage waveforms of different signals. Circuit operation is like this, initially capacitor C_{int} is discharged and all the capacitor are pre-

charged to V_{REF}. Then if bits associated with C_0 (LSB) and C_4 are '1' then the capacitors will switch to ground transferring charge to C_{int} once (at the positive going edge of ϕ_1) over the entire conversion cycle. Similarly capacitor pairs (C_1 C_5), (C_2 C_6) and (C_3 C_7) will push charge to C_{int} two times, four times and eight times respectively if the corresponding digital input bits are at logic level '1'. After eight-clock pulses the charge transfer is completed and the DAC reaches its final voltage. Then final voltage has the relation with the input digital signal

$$V_{out} = \frac{C}{16C_{\text{int}}} V_{REF}\left[2^{N-1}b_{N-1} + \ldots + 2b_1 + b_0\right] \quad \text{.....(Eqn 2.3.4.1)}$$

The final voltage is sampled and held by the sample-and-hold circuit for the next conversion cycle and the charge-integrating portion of the DAC prepares for next digital code to convert.

If flat array of same value capacitors [Figure. 2.3.2] architecture is used then the clock frequency required is $128f_S$, where f_S is the conversion frequency. But the two-stage architecture does the same operation with clock frequency $8f_S$. In other word for certain bandwidth of the op-amp the maximum conversion frequency becomes 8-times that of flat capacitor array. So we can say it is very good improvement almost without any cost.

Let us now look at all the proposed architectures to choose the best architecture. All the architectures have advantages and disadvantages. The binary-weighted reference voltage type DAC of Figure 2.3.1 converts digital input in one clock cycle. With this architecture high speed conversion of digital input is possible. But it suffers from severe problems. It requires N number of reference voltage sources having values V_{REF}, $2V_{REF}$.....$2^{N-1}V_{REF}$. The resolution of the DAC depends on the accuracy of the voltage sources. For high resolution DAC the sources should have highly accurate values. But it is not easy to design voltage sources with such precision over the entire voltage range from V_{REF} to $2^{N-1}V_{REF}$. Output voltage from a voltage source circuit generally varies with temperature. Non uniform temperature distribution will cause the deviation of the voltage output from actual value. That will give rise to non-zero DNL and INL.

Additionally, all these voltage sources take a fair amount of die area. So this architecture is not a good solution to the problems of binary-weighted SC DAC.

Next in queue is binary-weighted switching frequency DAC with same value of capacitor array [see. Figure 2.3.2a]. This architecture needs minimum value of capacitance. But main problem with this circuit is it requires the clock frequency, 2^{N-1}-times conversion frequency. The bandwidth of the charge integrating op-amp determines the maximum conversion frequency of the DAC. For proper response the unity gain frequency of the op-amp should be ~10 times the maximum clock frequency. So due to limited bandwidth of the op-amp the conversion frequency and the resolution of the DAC can not be very high. Complex digital block somewhat nullify the area improvement of the DAC. So this architecture also does not give a good solution.

The 3rd possibility is combination of the binary-weighted SC DAC architecture and binary-weighted switching frequency. It is much better solution compared to the first two possibilities. This is a solution between two extreme cases, one is pure binary-weighted capacitor single frequency architecture and other is pure binary-weighted frequency with same value capacitor architecture. It has the flexibility to satisfy different area requirement at the cost of speed of conversion.

The architecture with use of two-stage block of same value capacitors needs almost minimum value of capacitance, but there is a drastic improvement in terms of clock frequency and hence the speed of conversion. With this architecture an 8-bit DAC requires clock of frequency $8f_S$, instead of $128f_S$ required for a single array of capacitors of same value with binary weighted switching frequency. Since this architecture also needs capacitors of identical value, it enjoys better matching of the capacitors as does the binary-weighted frequency version architecture. This approach also provides the trading off facility between area and speed, which is provided by the combined architecture of Option 3.

Considering all these issues it can be said that the architecture with two-stage capacitor block of same value capacitor provides better solution to the huge area requirement of the binary-weighted SC DAC.

The order of matching accuracy of the capacitors remains same as that of a binary-weighted capacitor. And similar to binary-weighted SC DAC, its resolution is limited by the maximum DNL.

Chapter 3

Design of the D/A Converter

3.1 Introduction

This chapter deals with the design consideration of the different fundamental blocks of the DAC. Those are op-amps of the charge integrating circuit and the S/H circuit, CMOS transmission gate switch, 2-phase clock generator etc. The requirements of different blocks are different, like bandwidth requirement for both the op-amps are not same. The entire design problem is divided into two parts, one is design of analog building blocks and other is design of digital building blocks. Section 3.2 deals with analog circuit design and in the Section 3.3 design aspects of digital circuits are discussed. The layout issues are also explained in the last section of this chapter.

3.2 Analog Circuits:

Analog circuits are the most important building blocks of a mixed signal circuit. So most of the time is spent in dealing with analog circuits. Again the most important blocks among them are op-amps. Maximum care was taken in designing the op-amps. The sizes of the capacitors were chosen carefully so that the minimum sized capacitor does the job. Similarly switches were kept as small as possible not only to keep area small, but also mainly to keep error voltage due to clock feed through and charge pumping minimum. All of these issues are discussed in detail in the following sections.

3.2.1 Op-amp of Charge Integrating Circuit

One can say this is the heart of this DAC. Its performance mainly determines the performance of the DAC. The DAC's maximum conversion frequency is limited by the maximum achievable bandwidth of this op-amp. Care was taken to maximize the bandwidth keeping reasonable values of the gain and phase margin. The op-amp only drives the S/H circuit next to it. So high driving capability is not an important factor. A two-stage op-amp is used in the DAC. The schematic is shown in the Figure 3.2.1.1. In the input stage (M_5 and M_6) of the op-amp PMOS transistors are used to avoid the body-effect of the transistors and better power line noise immunity [discussed in the last portion of this section]. Because, the technology file [13] used for layout, only supports nwell. The design of an op-amp is not so easy task due to inter-dependency of the different parameters. The factors affect the circuit performance are gain, stability of the op-amp and unity gain frequency, slew rate of the etc.

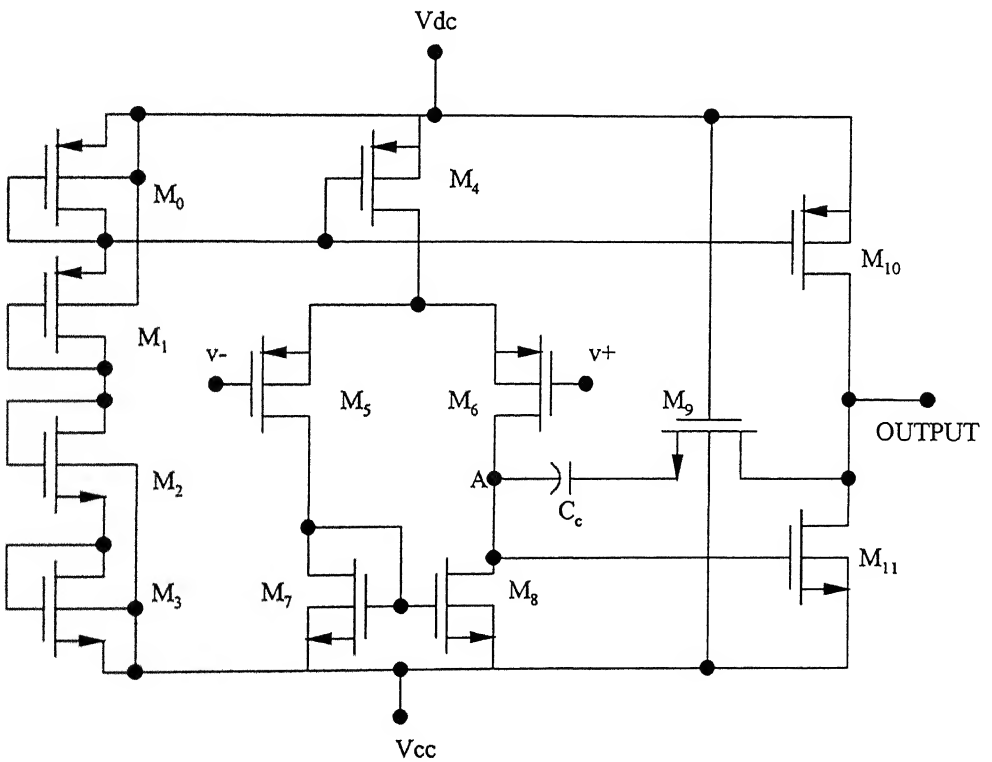


Figure 3.2.1: Two-stage Op-amp circuit with compensation.

Let us first consider the gain requirement. The integrator circuit in the Figure 3.2.2 is similar to the charge integration section of the DAC. Only difference is that here $V_{in} = V_{REF}$ (dc voltage). Still the transfer function is valid.

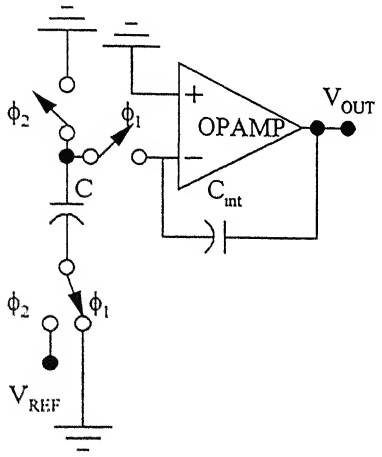


Figure 3.2.2: Stray insensitive non-inverting integrator.

The transfer function of the circuit with finite gain is [for detailed analysis see Ref.[3]]

$$H(z) = \frac{\left(C_1/C_2\right)\left[1+\left(1+C_1/C_2\right)/A_0\right]^{-1} z}{z-\left(1+1/A_0\right)\Big/\left[1+\left(1+C_1/C_2\right)/A_0\right]} \qquad \text{.....(Eqn. 3.2.1)}$$

Where A_0 is the gain of the op-amp. The ideal gain transfer function is

$$H(z) = \frac{\left(C_1/C_2\right)z}{z-1} \qquad \text{.....(Eqn 3.2.2)}$$

These two equations depict that finite gain of the op-amp reduces the gain of the circuit. So the final voltage at output is somewhat less than the ideal expected value. And it produces gain error of the DAC. For A_0>1000 (60 dB) the error is negligible. So the low frequency gain of the op-amp is chosen above 60dB. Longer length for transistors M_4, M_7 were taken. Longer channel length increases the load resistance of the input stage of the op-amp, which is necessary for large gain to achieve. As the large differential gain of an op-amp is necessary, the small common-mode gain is also equally important. The common mode gain depends on the output resistance of the bias current source (transistor M_8 acts as current source). For smaller common mode gain the channel length of the transistor M_8 was chosen 1.5μm, which is 2.5 times the minimum achievable length in 0.5μm technology.

The other two and most important design considerations are stability and slew rate of the op-amp. Compensation capacitor C_c was connected across the gain stage of the op-amp to ensure stability of the op-amp, when placed in the feed back circuit of the DAC. The small signal equivalent circuit of the op-amp is shown in the Figure 3.2.1.3. The capacitance C_A is the total capacitance at node A including the input capacitance of the gain stage of the op-amp. The pole of the transfer function due to the compensation capacitor was chosen well below the other poles of the transfer function. So effectively the op-amp has only one pole with the compensation. The pole determines the bandwidth of the op-amp and hence the maximum conversion frequency of the DAC. Since the trans-conductance of the differential stage is not so high due to low trans-conductance of the MOS transistors, zero of the transfer function comes down, which causes the deterioration of the gain margin and phase margin of the op-amp. The zero cancellation series R-C compensation was used to avoid the problem [3]. A biased NMOS transistor (M_9) was used as a resistor of R-C compensation circuit.

The sizes of transistors (M_{10} and M_{11}) of the second stage were chosen to ensure proper gain margin and phase margin. The (W/L) ratios of these two transistors became large and were biased to large current for large gain and phase margin.

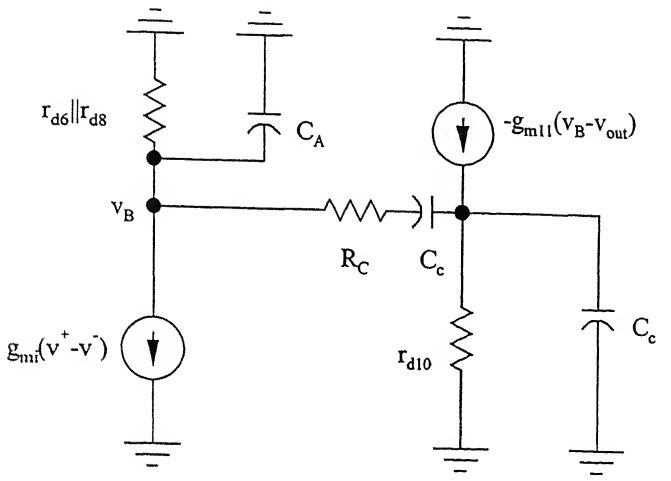


Figure 3.2.1.3: Small-signal equivalent circuit of the op-amp of Figure 3.2.1.1.

Since the output transistors are biased to large current, charging of the load capacitor (sampling capacitor of S/H stage) of the op-amp is not so critical. We can say that the slew rate of the op-amp is independent of the load capacitance. Then the slew rate of the op-amp totally depends on the bias current and the compensation capacitor. Bias current of the differential stage was chosen to achieve required slew rate. The expression for slew rate of the op-amp is

$$S_0 = \left|\frac{dv_{out}}{dt}\right| = \frac{I_{Bias}}{C_c} \quad \text{.....} (Eqn.3.2.3)$$

In worst case scenario the output of the op-amp can change from V_{dd} to zero (for input of all digital bits '1'). For 1MHz conversion rate the charging (or discharging) time of the compensating capacitor is ≈60ns. So required slew rate is S_0=55 V/μs. With 200fF compensation capacitor, the required bias current is 11μA. But the op-amp has positive going slew rate limitation of due to use of M_{10} as current source. To avoid the positive slew rate limitation the slew rate is taken $2.5S_0$. And so the bias current I_{Bias} is taken 25μA.

Apart from avoiding body effect, choosing PMOS transistors at the input stage has an additional advantage. The digital blocks use V_{dc} source as power line. And analog blocks use V_{dc} and V_{cc} sources. So noise in the V_{dc} power line is more than that of V_{cc}

power line. The noise gain entering through M_4 is common mode gain, which is small. And noise entering through M_{10} is added to the signal but the noise source has high impedance (because M_{10} acts as current source) and gets attenuated at high frequency by the load C_s of the S/H stage. So effective noise due to V_{dc} supply variation is attenuated [2]. But that is not true for noise entering through V_{cc}. If NMOS transistors were used in the input stage the op-amp will be more susceptible to noise in the V_{dc} power line, which is not desirable.

With 200fF-compensation capacitance the unity gain bandwidth was set 90MHz. To ensure that the circuit does not oscillate when it is placed in the feed back circuit, the gain-margin and phase-margin are properly set. The simulated results of different parameters of the op-amp are summarized in the Table 3.2.1.

Table: 3.2.1

Op-amp	Low Frequency Gain (dB)	Gain Margin (dB)	Phase Margin (in ^{0})	Unity-gain Frequency (MHz)	CMRR (dB)	Power-dissipation (mW)
Op-amp of the charge integrating circuit	63.8	20.1	61.3	89	≈80	2.12
Op-amp of the S/H circuit	65.1	31.04	82.6	23	≈80	1.1

3.2.2 Op-amp of S/H Circuit

The op-amp used in the S/H circuit is also of two-stage op-amp (schematic is same as Figure 3.2.1). This op-amp will drive the low pass filter following the DAC. The design parameters are different due to different bandwidth, slew rate requirements of this circuit. Since the clock frequency of the S/H circuit is $1/8^{th}$ of that of the charge integrating circuit, the unity gain bandwidth of this op-amp is well below that of op-amp of the charge integrating circuit. Other advantage of lower bandwidth is it reduces the

noise of the circuit, because thermal noise is directly proportional to the bandwidth of the circuit. The slew rate requirement is also less compared to that of the op-amp of the charge integrating circuit. The different parameter values of the op-amp are tabulated in the Table 3.2.1.

3.2.3 Sizing of the Transistors of CMOS Switches

The ON resistance of a switch must be as small as possible. And linearity of the switches is also a very important factor. But those things are not easy to achieve in this design due to contradictory design constraints. The smaller resistance value can be obtained by choosing large (W/L) of the transistor with minimum length transistor. But large W/L ratio creates the problem of more charge pumping and clock feed through (for detailed discussion, please see the last portion of this section).

The ON resistance of a CMOS switch is

$$R_{ON,CMOS} = \left[\mu_N C_{OX} \left(\frac{W}{L}\right)_N \left(V_{GS,N} - V_{T,N}\right) + \mu_P C_{OX} \left(\frac{W}{L}\right)_P \left(V_{SG,P} - |V_{T,P}|\right) \right] \quad ..(Eqn.\ 3.2.3.1)$$

A typical ON resistance variation of a CMOS switch is shown in the Figure 3.2.3.1.

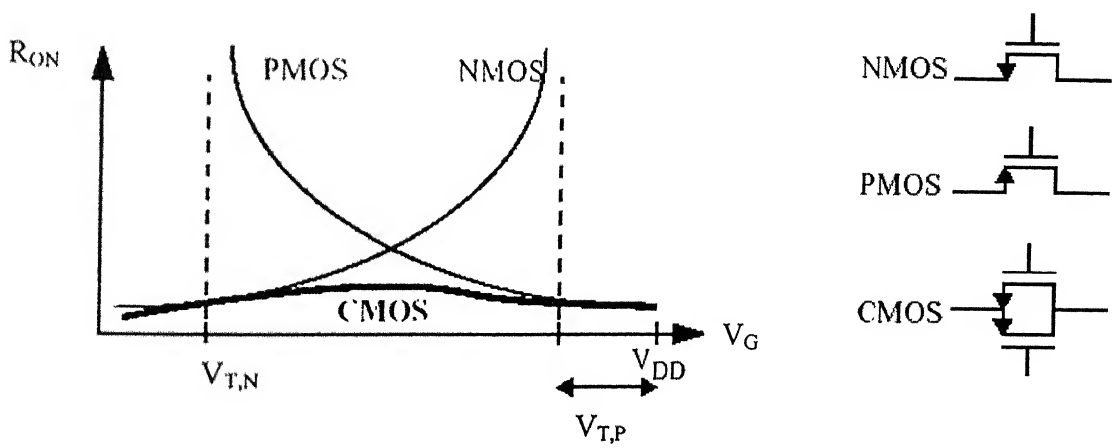


Figure 3.2.3.1: Variation of resistance of NMOS, PMOS and CMOS switches with in put signal level

The Figure 3.2.3.1 shows that the switch is more or less linear near the voltage $V_{dc}/2$. Different switches operate in different voltage ranges. For example switches to charge and discharge the charge pushing capacitors operate in ~0.7V to ground potential, the switches at the input of the charge integrating op-amp operates very close to ground potential, the RESET and SAMPLE switches operate from zero to V_{dc} potential. So linearity of the switches can not be ensured always. On the other hand for smaller resistance of the switches the W/L ratios of the transistors of the switches should be as large as possible. Simulation shows that non-linearity of the capacitor charging and discharging switches does not affect the circuit operation that much. Only it is to be ensured that the capacitor charges and discharges at the maximum operating clock frequency. The switches with minimum W/L=0.9μm/0.6μm are able to charge and discharge the capacitors at 50MHz clock-frequency, which is well above the maximum clock frequency. But proper sizing of other switches (at the input of charge integrating op-amp, RESET and at the input of S/H circuit) are very important. These switches are connected to high impedance node. And a slight charge injection to those nodes gets multiplied by the gain of the op-amp giving dc offset voltage at the output of the DAC.

For this switches not only the minimum resistance is to be ensured but the minimum value of error voltage has to be ensured. Before going to the actual design let us review the cause of error voltage due to charge pumping and clock feed through of an non ideal MOS switch and how it can be minimized.

When the switches are open the nodes are connected to low-impedance nodes and then there is no problem of charge pumping or clock feed through. But when the switches turn off then the problem comes. A MOS switch with NMOS and its lumped model are shown in the Figure 3.2.3.2. The analysis done below assumes a linear variation of the gate voltage V_G between V_{dd} and ground as shown in the Figure 3.2.3.2b.

The gate voltage at any time can be written as

$$V_G = V_{dd} - Ut \quad \text{.....(Eqn. 3.2.3.2)}$$

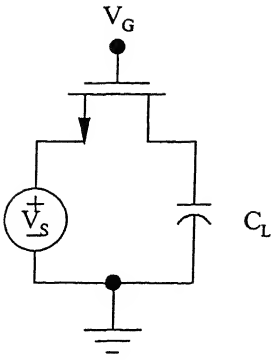


Figure 3.2.3.2a: Schematic of the switch circuit under study.

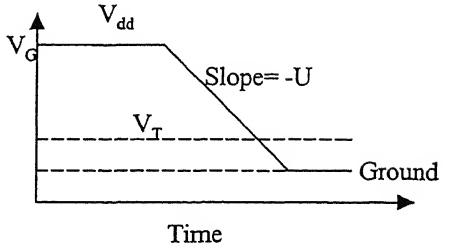
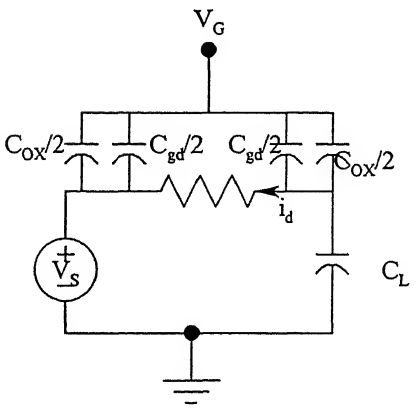
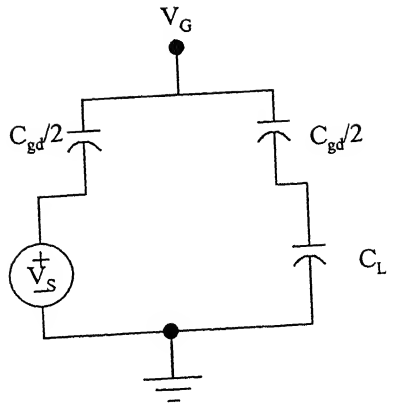


Figure 3.2.3.2b: variation of gate voltage.



(c)



(d)

Figure 3.2.3.2 (c) and (d): Equivalent lumped model for $V_{dd} \geq V_G \geq V_S + V_T$ and $V_S + V_T > V_G \geq 0$ respectively.

Generation of this error voltage occurs in two phases. First phase occurs in the gate voltage range

$$V_{dd} \geq V_G \leq V_T + V_S \quad \text{.....(Eqn 3.2.3.3)}$$

Where V_T is threshold voltage of the NMOS. Since the transistor are of minimum length we can assume that the transit time of the charges across the transistor is small compared to the fall time of the gate voltage and charge lost through substrate trap is negligible. As long as the channel is open underneath the gate of the transistor some of the charge of channel can pass to the low impedance node. But when the channel just turns off (at $V_G = V_T$) the entire the channel charge at that voltage is then divided into two parts, one part goes to the voltage source and other part goes to C_2. The charge on the C_2 causes error voltage on the capacitor.

Assuming that the transistor turns off for V_G just below the threshold voltage, the second phase occurs for

$$V_T + V_S > V_G > 0 \quad \text{.....(Eqn. 3.2.2.4)}$$

In the second phase there is no channel below the gate of the transistor and hence no effect of C_{OX}, only the gate-drain overlap capacitance (C_{gd}) contributes to the error voltage.

Combining both the effects the final error voltage can be written as [for detailed analysis please see. Ref [7]]

For slow-switching process,

$$\Delta V = \left(\frac{C_{gd} + \frac{C_{OX}}{2}}{C_L} \right) \sqrt{\frac{\pi U C_L}{2\beta}} + \frac{C_{gd}}{C_L}(V_S + V_T) \quad \text{.....(Eqn 3.2.2.5)}$$

Where

$$\beta = \mu C_{OX} \frac{W}{L}$$

And for fast-switching process is

$$\Delta V = \left(\frac{C_{gd} + \frac{C_{OX}}{2}}{C_L} \right) (V_{dd} - V_S - V_T) + \frac{C_{gd}}{C_L}(V_S + V_T) \quad \text{.....(Eqn 3.2.2.4)}$$

These equations show that error voltage greatly depends on the total oxide capacitance and gate-drain overlap capacitance C_{gd} and fast falling of gate voltage causes more error voltage and more the signal level V_S lower the error voltage [7][8]. From this analysis the conclusion can be drawn that for minimum error voltage C_{OX} and C_{gd} of the transistor must be minimum. To satisfy that condition W/L of the transistor should be minimum with minimum length L. And the fall time of the gate voltage should be as large as possible. Controlling the fall time of the gate voltage is a design aspect of the digital blocks.

The partial solution to reduce the error voltage is to use of CMOS switch [8]. So CMOS switch not only makes the switch linear over a voltage range but also reduces error voltage due to clock feed through and charge pumping. For small resistance transistors should have large W/L ratio on the other hand for minimum error voltage the transistor should have small W/L with minimum value of channel length. These are quite contradictory requirement. So some trade off was done to choose the W/L ratios of the transistors. Simulation shows that the switch resistance for the switches at the input of charge integrating op-amp and S/H circuit with minimum value of W/L =0.9μm/0.6μm ratio NMOS enough to get desired response. For cancellation of error voltage the W/L ratio of PMOSs were adjusted to 1.5μm/0.6μm. The switch of same size was taken for S/H circuit. The corresponding optimum values of W/L ratios of the transistors of the switch to discharge C_{int} were 3μm/0.6μm and 6μm/0.6μm.

3.2.4 Sizing of the Capacitors

This is another important design aspect of the DAC. Sizes of the capacitors directly affect die area consumed by the DAC. Ideally the capacitor value can be chosen as small as possible. But the parasitic capacitance, noise and error-voltage limit the minimum value of capacitance. Another matter, which limits the lower value of capacitance, is matching requirement of the capacitors.

In the designed DAC the stray insensitive switching scheme [1][3] was taken, that allowed the capacitor C to be chosen [Figure 2.3.1b] value even below 0.1pF. But the main limiting factor of choosing lower capacitance value is the matching requirement of the capacitances. As reported by J. Shyu et al [9], the cause of capacitor mismatch can be divided into two categories: one is systematic error and other is random error. Systematic error can be minimized by choosing proper matching techniques, like common centroid array of capacitors of unit cells. The control of random error is not in designer's hand. So ultimately it limits the matching accuracy of capacitors. It random error has four main parts. They are edge variation and oxide variation for local and global effects. Assuming all of these effects are independent, combined relative capacitance error for a single plate capacitor can be expressed as [9]

$$\frac{\Delta C}{C} = \sqrt{k_{le}C^{-\frac{3}{2}} + k_{ge}C^{-1} + k_{lo} + k_{go}} \quad \text{.....} (Eqn 3.2.4.1)$$

Where k_{le} is the local edge effect factor, k_{ge} is the global edge effect factor, k_{lo} is the local oxide factor and k_{go} is the global oxide factor. All are function of their respective standard deviation [9]. It is also reported in the paper that for 1:1 capacitor ratio and C=0.316pF in 3.5μm technology, the accuracy of matching of the order of 0.1% can easily be obtained. The matching accuracy is slowly varying function of capacitance ratio. The dominant error sources of capacitor mismatch are global edge effect and global oxide effect [9].

The HP0.5 technology chosen for implementation of DAC provides a separate well, called capacitor well for linear capacitor fabrication [12]. The linear capacitor fabricated in capacitor well has large capacitance per μm^2 (2.24fF) [12]. Large capacitors can be obtained with smaller area. This reduces the global error effects on capacitor mismatch. The required accuracy of 8-bit DAC is 0.4% which can easily be obtained. Considering the matching accuracy requirement the capacitance of value 0.15pF was taken for charge pushing capacitors. But for the charge integrating capacitor C_{int} and capacitor of the S/H circuit (C_S) the situations are different. The error voltages on these capacitors are inversely proportional to the corresponding capacitance values [see Section 3.3.2]. The capacitance values should be as large as possible from minimum error voltage point of view. Higher value of capacitance also lowers noise the generated in the capacitance, because the noise generated in a capacitance (C) is also inversely proportional to C. C_{int}= 0.6pF and C_S=0.15pF were chosen to keep error voltage well below the ½ LSB of the DAC.

3.3 Digital Circuits

The digital design is much easier than that of analog circuits. The digital block contains 2-phase clock generator, digital frequency divider and combinational block to generate different switching signals. The design issues of the digital blocks are discussed here.

3.3.1 Two-phase Clock Generator

As discussed in Section 2.3, the DAC needs a 2-phase non-overlapping. Shown in Figure 3.3.1a is the schematic of the 2-phase clock and Figure 3.3.1b illustrates the waveforms (ϕ_1 and ϕ_2) two phases of the clock. The one of main requirements of the 2-phase clock is the non-overlapping potion should be larger than the maximum difference in the delay of ϕ_1 and ϕ_2 in different paths. The first requirement ensures the condition "Break before make" of the switches. And other important requirement is the fall time of the clock should be as large as possible. Second condition gives minimum error voltage due to clock feed through and charge-pumping effects of a non-ideal switch. The error voltage is function of fall time of the clock (discussed in the section 3.2.3). To make fall time large, the driving stages (NOT gates) of the clock were kept smaller sized. The inverted clocks to drive PMOSs of the switches were generated by NOT gates of same size of that of the driving stage.

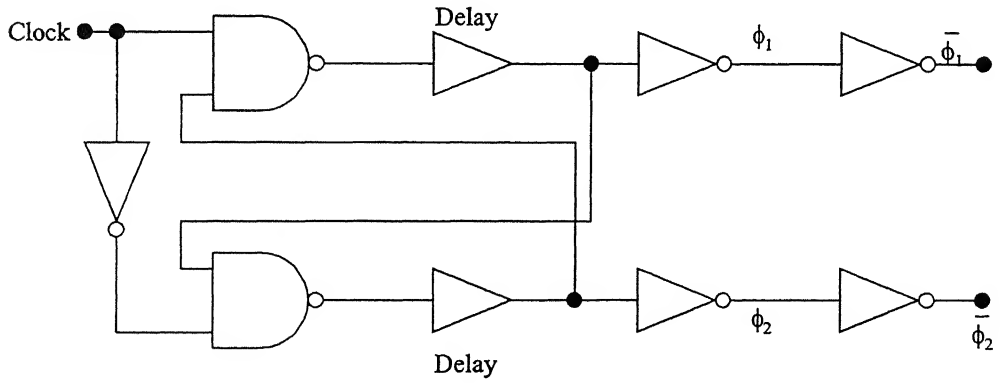


Figure. 3.3.1a: 2-Phase Clock Generator

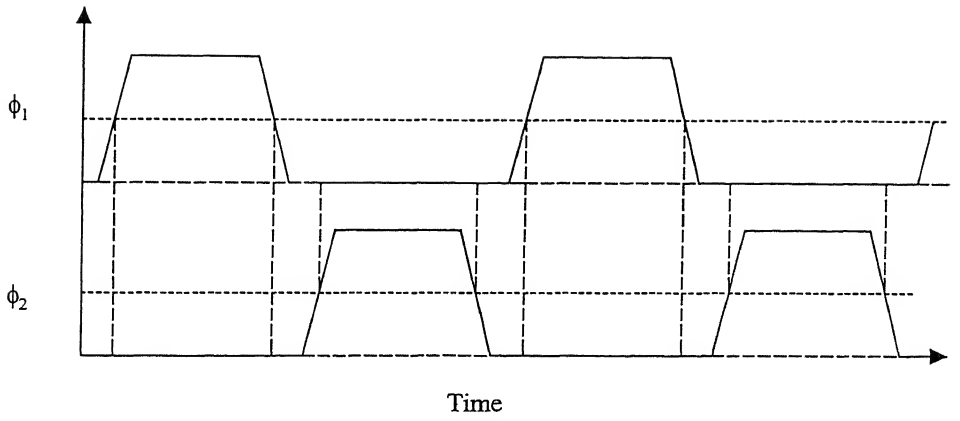


Figure: 3.3.1b: Waveform of 2-phase clock.

3.3.2 Other Digital Blocks

The other digital blocks are digital frequency divider, and combinational block to generate different switching signals. Those were implemented with different logic gate with minimum area constrain. Simulation shows that with minimum area constraint the propagation delays of different signals are enough to get the proper operation of the DAC.

3.4 Layout

The DAC was laid out using Cadence Virtuoso-layout editor. DRC and extractions of the layout were done with the same CAD tool. The technology file [13] of fabrication process 0.5HP was used to set up the technology library. The entire DAC was laid out by hand. The full custom design makes the circuit compact. Before going for the final layout, floor plan was done keeping many issues in mind. Those issues are discussed below.

1) The analog circuitry was categorized by the sensitivity of the analog signal to noise. For example, the inverting input node of the charge integrating op-amp and non-inverting input of op-amp of S/H circuit [Figure 2.3.5a] are very sensitive to noise. So these blocks are considered as maximum noise sensitive analog blocks. Bottom plates of the charge pushing capacitors and the transmission gate switches are connected to low impedance nodes (either V_{REF} or ground). So they are comparatively less noise sensitive

analog blocks. Similarly the digital circuitry are also categorized by their switching speed. Two-phase clock generator and digital frequency divider operate at very high frequency and on the other hand the control logic signal generator operates comparatively at lower frequency.

The noise sensitive analog blocks were placed farthest from the high-speed digital blocks to reduce digital switching noise. In between them low speed digital blocks and less sensitive analog blocks were placed.

2) Separate Guard rings were used around the noise sensitive analog blocks (both the op-amps) and digital blocks. That reduces the coupling capacitor between those blocks and hence the cross-talk through the substrate.

3) The sensitive interconnect, like connection from the capacitor block to the switches at the inverting input of the charge integrating op-amp were properly shielded with analog ground line.

4) Running interconnect containing sensitive analog signals parallel and adjacent to any interconnect carrying digital signals were avoided. This reduces the coupling of analog signal with digital switching noise.

5) The total interconnect length was tried to keep minimum.

And finally,

6) The area of the complete DAC was also tried to keep minimum.

Considering all these issues the different cells are placed. And the final floor plan of the complete DAC is shown in the Figure 3.4.1. And the final layout with the labeling of different blocks are shown in the Figure 3.4.2.

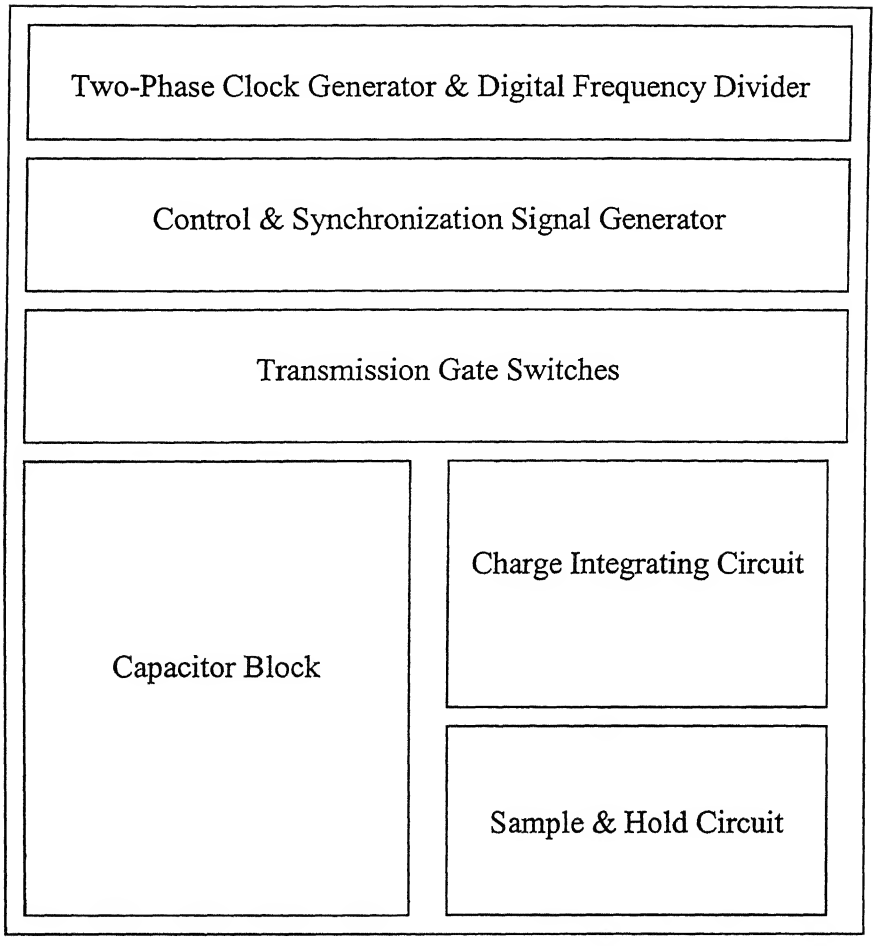


Figure 3.4.1: Final floor plan of he complete DAC.

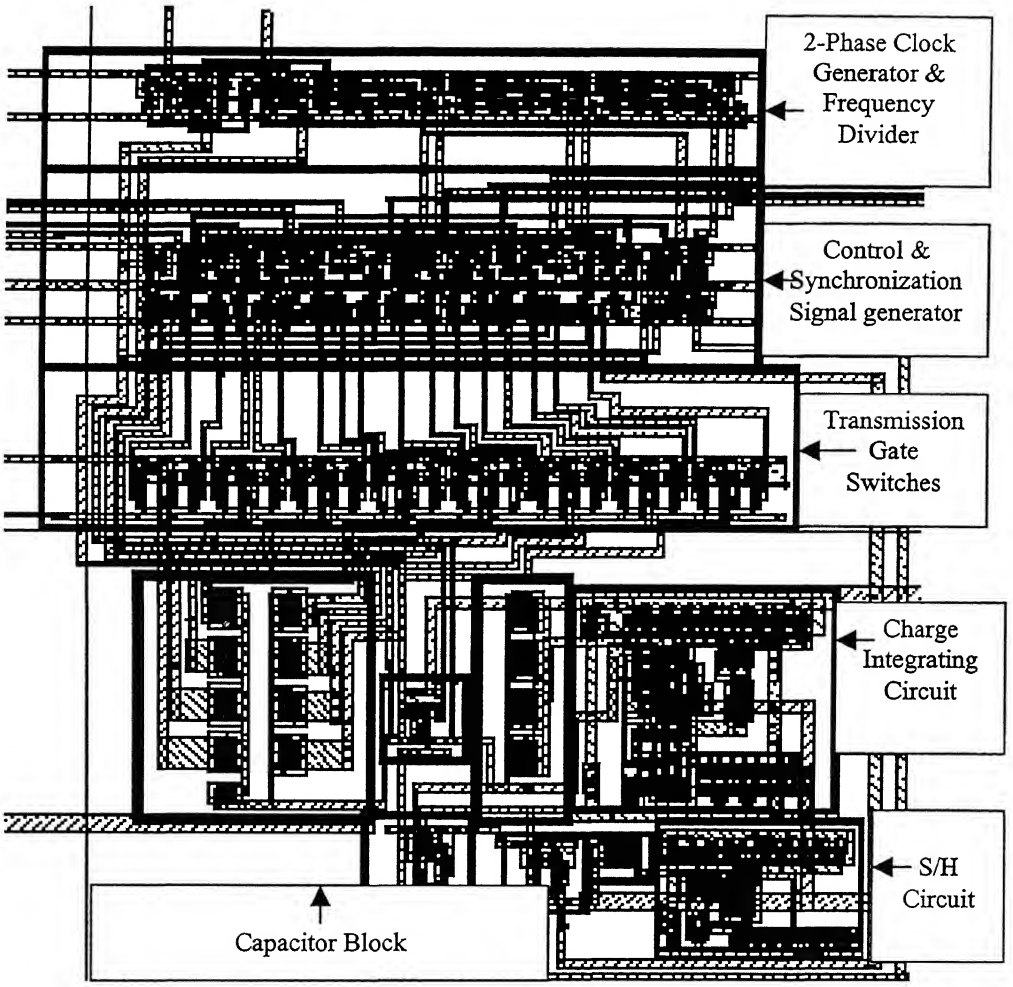


Figure 3.4.2: Layout of the D/A converter

Chapter 4

Results and Discussions

4.1 Introduction

First the individual functional blocks are laid out in 0.5HP (0.5μm single-poly, 3 metal with capacitor well for linear capacitor fabrication) CMOS fabrication process. Then the circuit was extracted from the layout. The functionality of the individual block was conformed with the simulation of the extracted circuit. It was sometimes found that the extracted circuit was not giving expected results due to parasitic capacitors in the extracted view, then the circuit was redesigned. It was tried to solve the problem at as low level of the hierarchy as possible. When the functionality of the individual blocks were satisfactory, then the individual blocks were integrated to get the final layout of the DAC. Again the circuit of the entire DAC was extracted from the integrated layout. And the operation of the DAC was tested with the simulation. The Spectre simulator of Cadence Affirma@ Analog Circuit Design Environment CAD tool was used for all the simulations. In this chapter different simulated results of the DAC are discussed.

4.2 DAC Output

There are 256 combinations of the input digital bit of an 8-bit DAC. So there are 256 different level of analog voltages. Since it is linear DAC, each voltage levels are equally separated. Here in the Figure 4.2.1 only 16 output voltage levels are shown for input bit combination having decimal equivalents from 0 to 15. The ideal step height

(LSB) of the DAC is 9.375 mV. The waveform shows that it faithfully produces analog output of corresponding digital input. The DAC has 250μV off voltage. The main source of the offset voltage is the clock feed through.

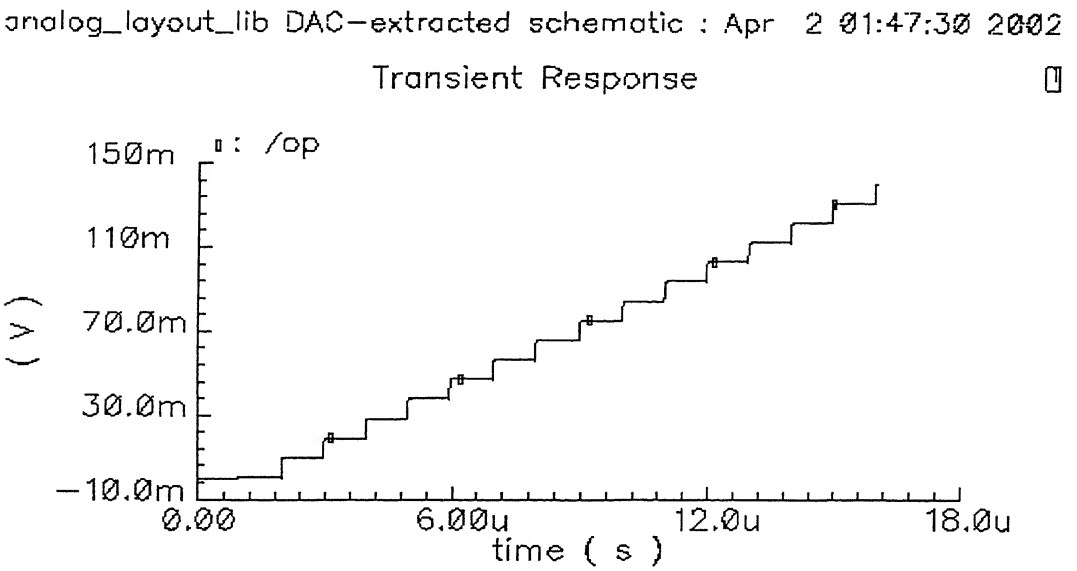


Figure 4.2.1: DAC output.

In every clock pulse the switches at the input of the charge integrating op-amp transfer some amount of charge causing error voltage on the capacitor C_{int}. After every 8-clock pulse the output is sampled. Even if all the input bits are '0', due to the accumulated error voltage, some offset voltage comes at the output. This problem can be solved with fully differential design of the charge integrating circuit.

4.3 INL and DNL Plot

The simulation was done with 8 MHz clock. The conversion frequency of the DAC at that clock frequency is 1MHz. Figure 4.3.1 and Figure 4.3.2 show that both DNL and INL are below ½ LSB. And the DAC shows good linearity over the entire voltage range. In the simulation the capacitors were assumed to be ideal. Only source of non-zero INL and DNL are parasitic capacitance at different nodes. Though the circuit is almost insensitive to the parasitic capacitance at the virtual ground node, but it is sensitive to the parasitic capacitance at the other terminal of the charge attenuating capacitor C_{attn}.

parasitic capacitance at the virtual ground node, but it is sensitive to the parasitic capacitance at the other terminal of the charge attenuating capacitor C_{attn}. Increasing the value of the capacitor associated to each bit, the effect of parasitic capacitance can be reduced.

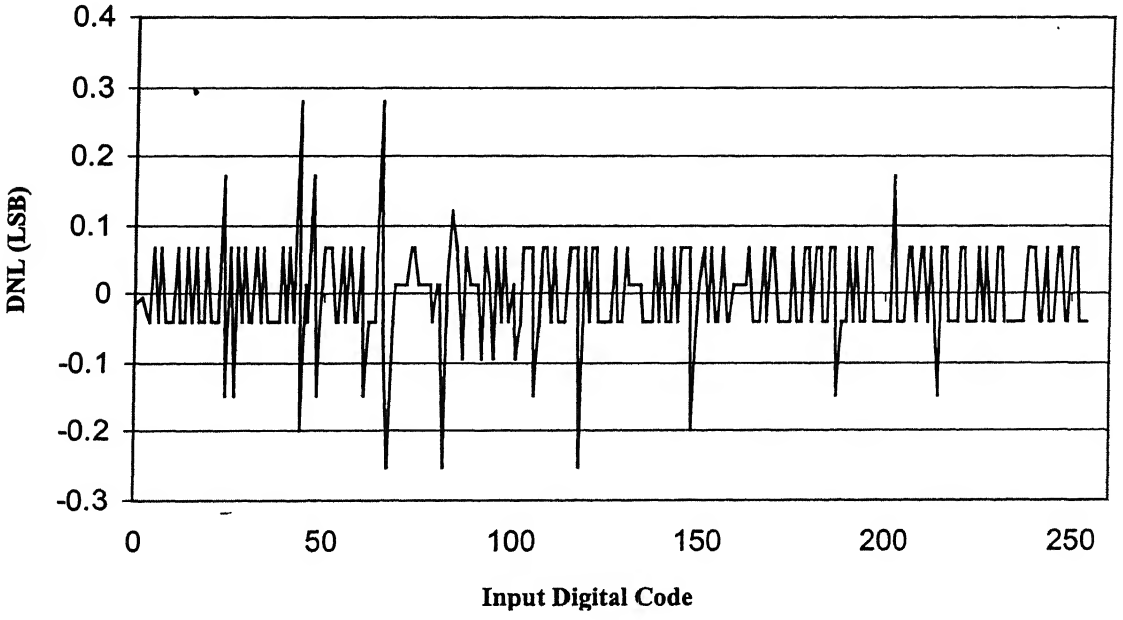


Figure 4.3.1: The simulated result of D/A converter's differential non-linearity.

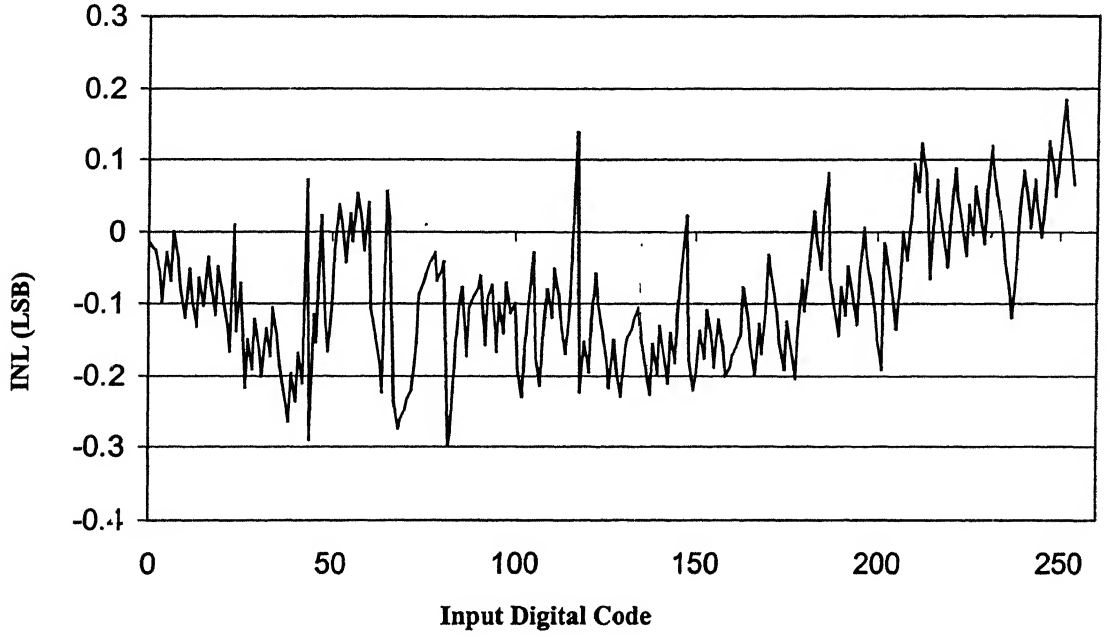


Figure 4.3.2: The simulated result of D/A converter's integral non-linearity.

In actual circuit there is capacitor mismatch. This will give higher INL and DNL. To keep the INL and DNL below ½ LSB the capacitors should be very accurately matched. The order of

accuracy is determined by the capacitor associated with the MSB. The capacitor associated with the MSB must have least amount of capacitor mismatch. Because it transfers charge 8 times over a complete conversion cycle and mismatch also gets multiplied by 8 times.

4.4 Area Taken by Different Blocks of the DAC

The area taken by different blocks of the DAC are summarized in the Table 4.4.1 below.

Table 4.4.1

Area Taken by Different Blocks of the DAC

Two-phase clock & Freq. Divider block (in μm^2)	Control signal and synchronization signal generator (in μm^2)	Transmission gate switch block (in μm^2)	Capacitor block (in μm^2)	Charge integrating Circuit (in μm^2)	Sample & Hold circuit (in μm^2)
6,600	9,000	7,050	25,500	9,000	6,250

In a binary-weighted capacitor SC DAC the capacitor block takes most of the space. But The Table 4.4.1 shows that though area taken by the capacitor block is still grater than all other blocks, but they are now of the same order.

4.5 Comparative Study of Capacitance Area Taken by the designed DAC with That of Binary-weighted DAC

First capacitance area of an eight-bit binary-weighted SC DAC and that of a two-stage binary weighted DAC are estimated considering same minimum capacitor value C. The results are given with the area taken by capacitor block of the designed DAC in the Table 4.5.1.

Table 4.5.1

Comparison of capacitor values and frequency requirements of proposed DAC with Binary-weighted SC DAC and Two-stage binary-weighted SC DAC

Resolution of the DAC (in bits)	Capacitor Value required for the proposed DAC architecture	Clock frequency required for the proposed DAC architecture	Capacitor Value required for Binary-weighted SC DAC	Capacitor Value required for Two-stage binary-weighted SC DAC
8	8C	$8f_S$	255C	30C
10	10C	$16f_S$	1023C	62C
12	12C	$32f_S$	4095C	126C

From the Table 4.5.1 it is clear that for an 8-bit DAC ~22 times the capacitor value of the proposed DAC is required for Binary-weighted SC DAC and ~3.7 times is required for two-stage binary-weighted DAC. Similarly, for 10-bit they are ~102 and 6.2 times and for 12-bit 341 and 10.5 times respectively. But the clock frequency requirement of the new architecture for 8,10 and 12-bit DAC are $8f_S$, $16f_S$ and $32f_S$ respectively, where f_S is the conversion frequency. So, these results give the actual picture of how much of space is saved with this new architecture at the cost of speed of operation.

4.6 Maximum Frequency of Operation

The maximum frequency of operation mainly limited by the finite unity gain frequency of the charge integrating DAC. As the clock frequency increases the output of the charge integrating circuit does not get enough time to rise to the final steady state voltage. This gives rise to deviation of the output from expected value giving rise to higher INL and gain error of the DAC. In worst case situation the all the input may change between all bits '0' to all bits '1' in every conversion cycle. Then the output waveform becomes train of square pulses. Even under worst case condition the two levels of the output voltage should be within ½ LSB range of the expected value. The waveform with 16MHz clock (2MHz conversion frequency) under worst case situation (defined earlier) is shown in the Figure 4.6.1. Under this condition the INLs for both the levels are nearly equal to 0.53LSB. So maximum conversion frequency of the DAC is 2MHz.

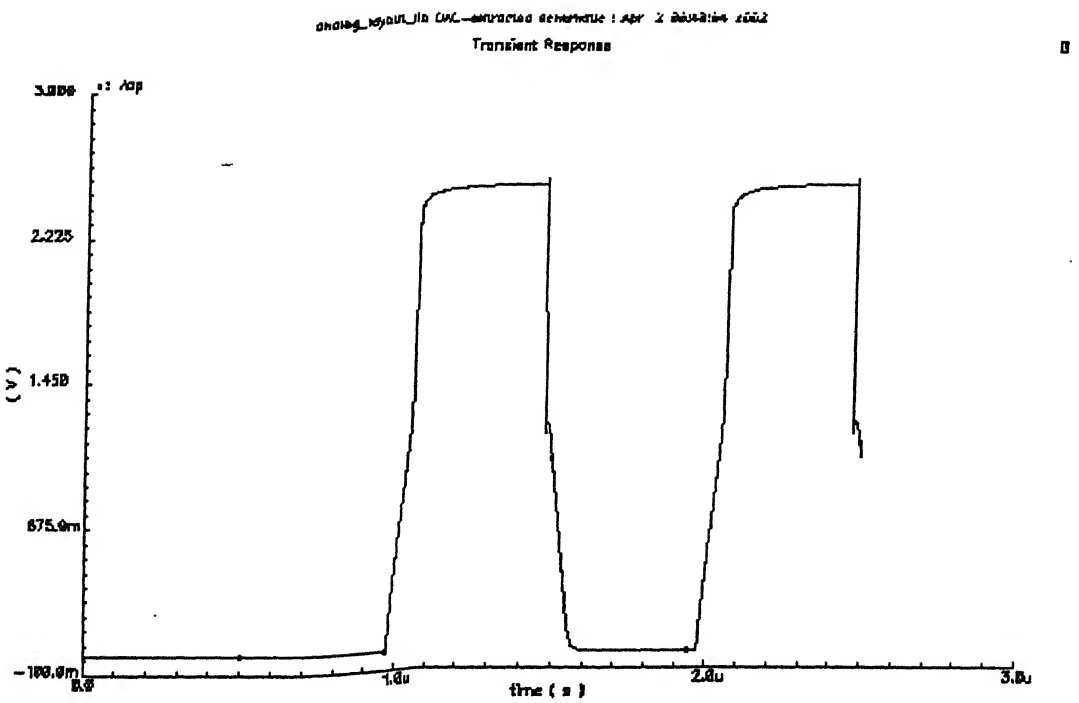


Figure 4.6.1: Output waveform with 16MHz (2MHz-conversion frequency) clock and all the input bits are simultaneously changing between '0' and '1'.

Chapter 5

Conclusions

5.1 Conclusions

Switched-capacitor digital-to-analog converter with binary-weighted capacitor array suffers from the disadvantage that the area required to fabricate the capacitors doubles with each additional bit of resolution. There are various possibilities to solve the large area requirement of the binary-weighted SC DAC. Each of them has advantages and disadvantages. In this work, a modified architecture is proposed, which overcomes this disadvantage by using the same value of capacitor for each bit of the DAC. This is achieved by trading the frequency of operation for the area of the DAC. Considering all the advantages and disadvantages, it can be said that, the proposed architecture gives a better solution to the problem. Simulated results for the proposed architecture for 0.5μm CMOS technology show INL and DNL less than 0.3LSB at a conversion frequency greater than 1MHz.

5.2 Future Work

The dynamic rage of the DAC can be increased one bit without any additional capacitor just using few XOR gates as done in the literature [5]. This DAC suffers from monotonicity problem. This problem can be reduced by using modified architecture

shown in the Figure 5.2.1, at the cost of more complex digital block.

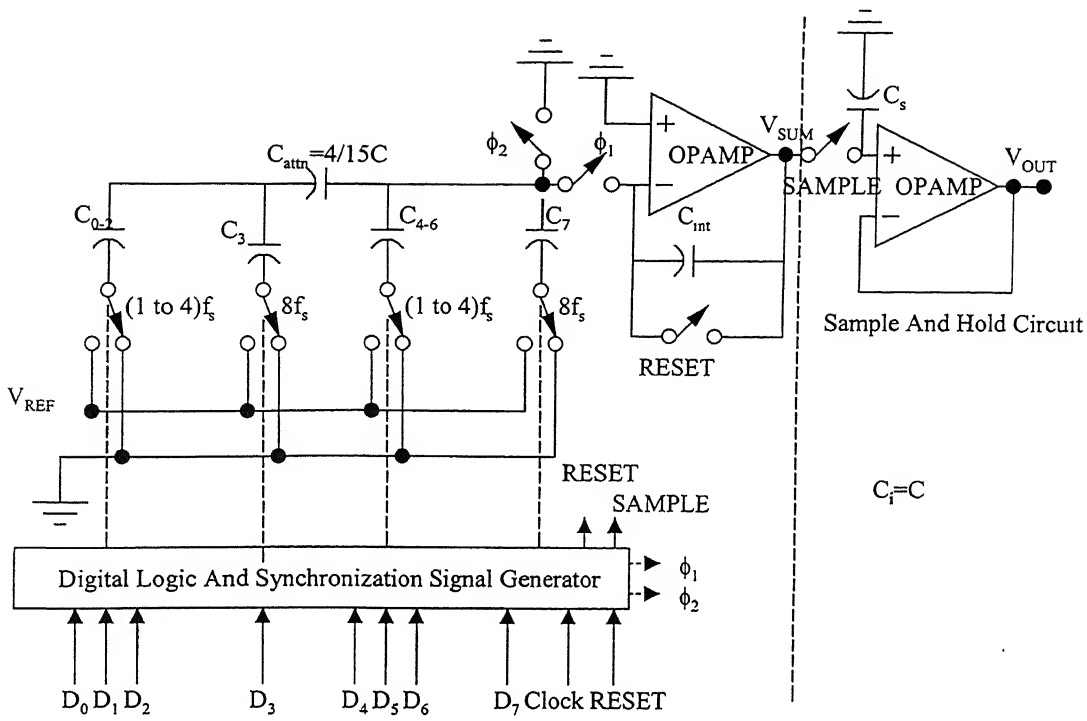


Figure 5.2.1: Proposed modified architecture to improve monotonicity of the designed DAC

The digital switching signal can be generated such that number of switching pulse to the capacitor C_{0-2} is equal to the magnitude of the binary code represented by bits $D_0D_1D_2$. When all the bits are '1' then it will send maximum seven clock pulses. Similar switching strategy can be used for capacitance C_{4-6} with $D_4D_5D_6$ bits. And the switching signal to the C_3 and C_7 are same as that of designed DAC. When all bits of $D_0D_1D_2$ are '1' then same capacitor will switch seven times, so from $D_0D_1D_2$ = 000 to 111 the output will remain monotonic. It is also true for $D_4D_5D_6$ bits. So with this architecture the monotonicity of the DAC can be improved.

Additional advantage of this architecture is, it requires less number of capacitor. That improves the matching of the capacitor because less global error effects [9].

Appendix A: Binary Code and Its Corresponding Thermometer Code

The thermometer code for 4 bit binary code with corresponding decimal value is given in the Table A.1.

Table A.1

Binary Code Digital and its Corresponding Thermometer Code

Decimal	Binary	Thermometer
0	0000	000000000000000
1	0001	000000000000001
2	0010	000000000000011
3	0011	000000000000111
4	0100	000000000001111
5	0101	000000000011111
6	0110	000000000111111
7	0111	000000001111111
8	1000	000000011111111
9	1001	000000111111111
10	1010	000001111111111
11	1011	000011111111111
12	1100	000111111111111
13	1101	001111111111111
14	1110	011111111111111
15	1111	111111111111111

From the table it is clear that one LSB change in binary code corresponds to one bit change in thermometer code. Thermometer code requires 15 bits to represent 4-bit binary word. Similarly 2^N-1 bits are required to represent an N bit binary word.

Appendix B: Calculation of Integral and Differential non-linearity of a Binary-weighted SC DAC

Integral non-linearity (INL) and differential non-linearity (DNL) of DAC is a measure of linearity of the DAC. Non-zero INL and DNL come due to the mismatch of the passive components of a DAC. Let us calculate INL and DNL error of a binary weighted SC DAC due to mismatch in capacitor value. First consider capacitor associated with k^{th} bit of the digital input deviates ΔC_k amount from the ideal value, then the capacitance of the k^{th} capacitor of the capacitor array is [Figure A.]

$$C_k = 2^{k-1}C + \Delta C_k \quad for\ k = 0,1,2....N-1 \quad .....(Eqn.\ B.1)$$

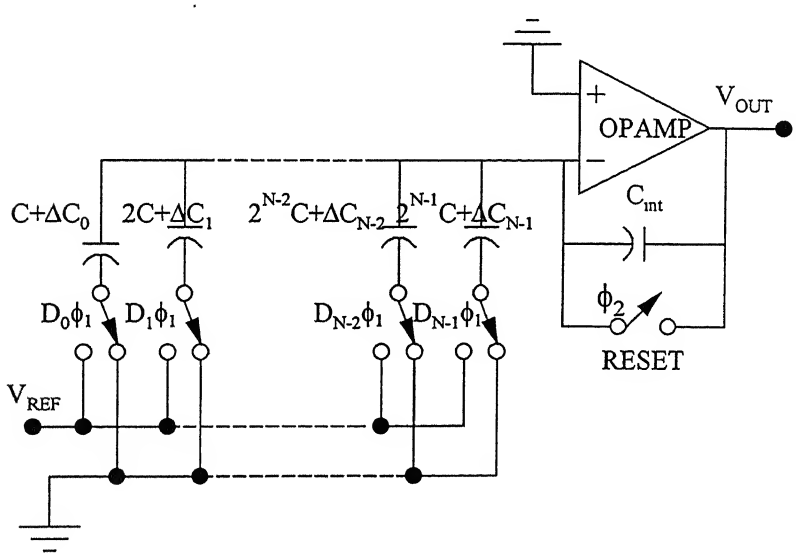


Figure B.1: Binary-weighted capacitor SC DAC with capacitor mismatch.

And with another assumption, capacitor corresponding to MSB has maximum positive mismatch error and remainder of the bits contains a maximum negative mismatch error, that is

$$\sum_{k=0}^{N-1} \Delta C_k = 0 \quad .....(Eqn.\ B.2)$$

Now the general expression for INL is

$$INL = V_{n,actual} - V_{n,ideal} \quad \text{.....(Eqn. B.3a)}$$

Where $V_{n,actual}$ is the actual analog output voltage for a certain input code n and $V_{n,ideal}$ ideal voltage for that input code. For a N bit DAC there will be 2^N number of input code from all bits '0' to all bits '1'.

The INL in terms of LSB can be written as

$$INL = \frac{V_{n,actual} - V_{n,ideal}}{LSB} \quad \text{.....(Eqn. B.3b)}$$

LSB is the smallest possible change in the analog output voltage.

Again for binary-weighted capacitor SC DAC the value of LSB is

$$LSB = \frac{C}{C_{\text{int}}} V_{REF} \quad \text{.....(Eqn B.4)}$$

Worst case INL of a DAC determines the INL of the DAC. Now under the assumption of (Eqn. B.2) the worst case INL occurs at the mid-code, where the MSB of the input digital code is '1' and all other bits are '0'.

For that input combination the expected ideal analog voltage is

$$V_{n,ideal}\Big|_{INL,\max} = \frac{2^{N-1}C}{C_{\text{int}}} V_{REF} \quad \text{.....(Eqn. B.5)}$$

And the actual output in presence of capacitor mismatch the analog output can be written as

$$V_{n,actual}\Big|_{INL,\max} = \frac{2^{N-1}C}{C_{\text{int}}} V_{REF} \quad \text{.....(Eqn. B.6)}$$

So the worst case INL becomes of the form given below

$$|INL|_{\max} = \frac{2^{N-1}C + |\Delta C|_{\max,INL} - 2^{N-1}.C}{C_{\text{int}}} .V_{REF} = \frac{|\Delta C|_{\max,INL}}{C_{\text{int}}} V_{REF} \quad \text{.....(Eqn. B.7)}$$

Similarly, the general expression for differential non-linearity is

$$DNL = \left| V_{n-1,actual} - V_{n,actual} \right| - LSB \quad \text{.....(Eqn. B.8)}$$

The worst case DNL occurs when MSB switches from 0 to 1 and rest of the bits switches from 1 to 0 and vice versa.

So when MSB is '1' and all other bits are '0' then the actual analog output is

$$V_{n,actual} = \frac{2^{N-1}C + \Delta C_{N-1}}{C_{\text{int}}} V_{REF} \quad \text{.....(Eqn. B.9a)}$$

And the expression for $V_{n-1,actual}$ is

$$V_{n-1,actual} = \frac{\sum_{k=0}^{N-2}\left(2^k C + \Delta C_K\right)}{C_{\text{int}}} V_{REF} \quad \text{.....(Eqn.B.9b)}$$

The assumption in the (Eqn. B.2) implies that

$$\sum_{k=0}^{N-2} \Delta C_k = \Delta C_{N-1} = \left|\Delta C\right|_{\max} \quad \text{.....(Eqn. B.10)}$$

So the worst case DNL can be written as

$$DNL_{\max} = \frac{\left[2^{N-1}C + \left|\Delta C\right|_{\max,DNL} - \left(\sum_{k=0}^{N-2} 2^k C - \left|\Delta C\right|_{\max,DNL}\right)\right] - C}{C_{\text{int}}} V_{REF} = \frac{2\left|\Delta C\right|_{\max,DNL}}{C_{\text{int}}} V_{REF}$$

.....(Eqn. B.11)

The maximum value of DNL and INL should be less than ½ LSB.

Appendix C: W/L Ratios of Different Transistors of the Op-amps

W/L ratios of the op-amp of the charge-integrating circuit and of S/H circuit with their corresponding values of compensation capacitors are tabulated in the table below:

Table C.1

W/L ratios and the values of compensation capacitors for both the op-amp

Op-amps =>	Op-amp of the Charge integrating circuit	Op-amp of the S/H circuit
M_0 (in μm/μm)	3.5/0.6	3.5/0.6
M_1 (in μm/μm)	3.5/0.6	3.5/0.6
M_2 (in μm/μm)	0.9/3.0	0.9/3.0
M_3 (in μm/μm)	0.9/3.0	0.9/3.0
M_4 (in μm/μm)	15.0/1.0	6.0/1.0
M_5 (in μm/μm)	10.0/1.0	5.0/1.0
M_6 (in μm/μm)	10.0/1.0	5.0/1.0
M_7 (in μm/μm)	20.8/1.0	8.4/1.0
M_8 (in μm/μm)	20.8/1.0	8.4/1.0
M_9 (in μm/μm)	30.0/0.6	10.0/0.6
M_{10} (in μm/μm)	70.0/0.6	26.0/0.6
M_{11} (in μm/μm)	70.0/0.6	26.0/0.6
C_c (in fF)	150	250

Appendix D: Block Diagram of Frequency Divider and the Gate Net-list of the Control and synchronization Signal generator

The frequency divider circuit was implemented with master-slave flip-flops in toggle mode. The frequency divider schematic is shown in the Figure D.1. It is of ripple

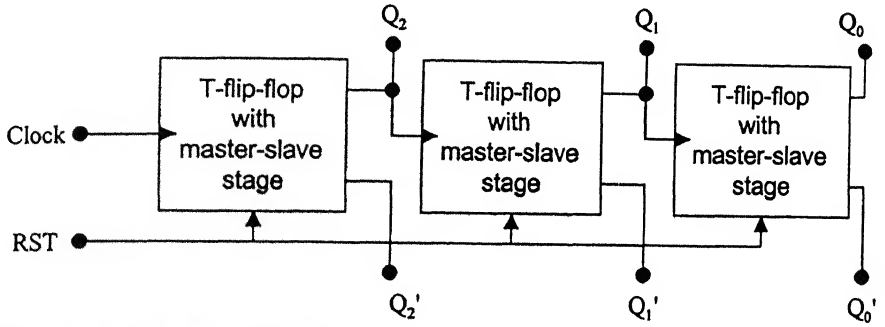


Figure D.1: Digital frequency divider

counter type. The control signals required for the proper operation of the proposed DAC architecture are summarized in the Table D.1 with their corresponding Boolean expression. CRGs and DCRGs are the signal required to charge and discharge the capacitors respectively, associated with the different bits (from D_0 to D_7) of the input digital signals. Capacitor charging and discharging network with transmission-gate switches of a capacitor for i^{th} bit is shown in the Figure D.2. CRG and DCRG are non-overlapping in nature. Other control signals, RESET is required to discharge the charge-integrating capacitor and SAMPLE is required for S/H circuit.

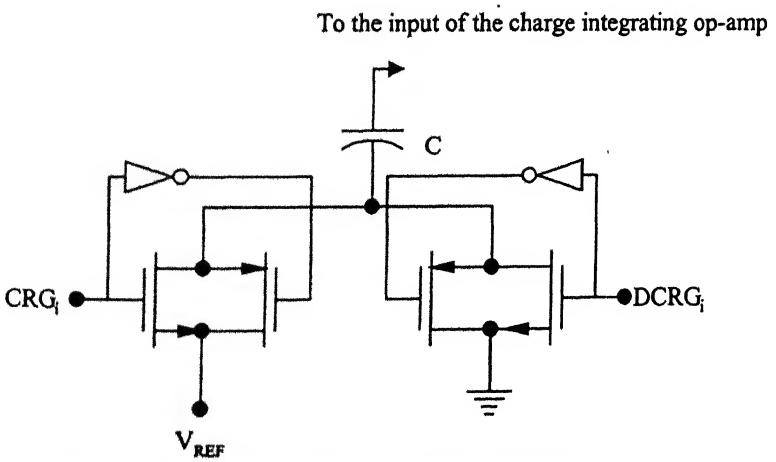


Figure D.2: Capacitor charging and discharging network associated with i^{th} bit of the input digital word with transmission gate switches.

Table D.1
Boolean expressions for different control signals

Input bit	Control Signals	Boolean Expression	Input bit	Control Signals	Boolean expression	RESET (Boolean expression)	SAMPLE (Boolean expression)
D_0	CRG_0	$D_0Q_2Q_1'Q_0\phi_1$	D_4	CRG_4	$D_4Q_2Q_1'Q_0\phi_1$	$Q_2'Q1'Q_0'\phi_2$	$Q_2Q_1Q_0\phi_1$
	$DCRG_0$	$(D_0Q_2Q_1'Q_0\phi_2)'$		$DCRG_4$	$(D_4Q_2Q_1'Q_0\phi_2')'$		
D_1	CRG_1	$D_1Q_2Q_1'\phi_1$	D_5	CRG_5	$D_5Q_2Q_1'\phi_1$		
	$DCRG_1$	$(D_1Q_2Q_1'\phi_2')'$		$DCRG_5$	$(D_5Q_2Q_1'\phi_2')'$		
D_2	CRG_2	$D_2Q_2'\phi_1$	D_6	CRG_6	$D_6Q_2'\phi_1$		
	$DCRG_2$	$(D_2Q_2'\phi_2')'$		$DCRG_6$	$(D_6Q_2'\phi_2')'$		
D_3	CRG_3	$D_3\phi_1$	D_7	CRG_7	$D_7\phi_1$		
	$DCRG_3$	$(D_3\phi_2')'$		$DCRG_7$	$(D_7\phi_2')'$		

The gate net-list of the control and synchronous signal generator is shown in the Figure D.3. Its inputs are come from the two-phase clock generator, the frequency divider and the data inputs D_0-D_7.

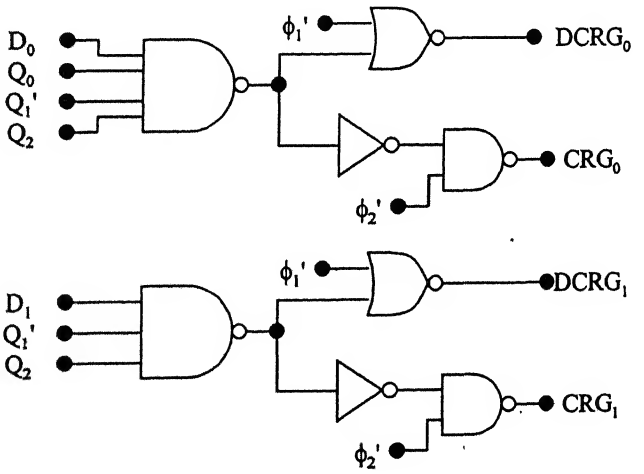


Figure D.3: Gate netlist of control and synchronization signal generator (continued...)

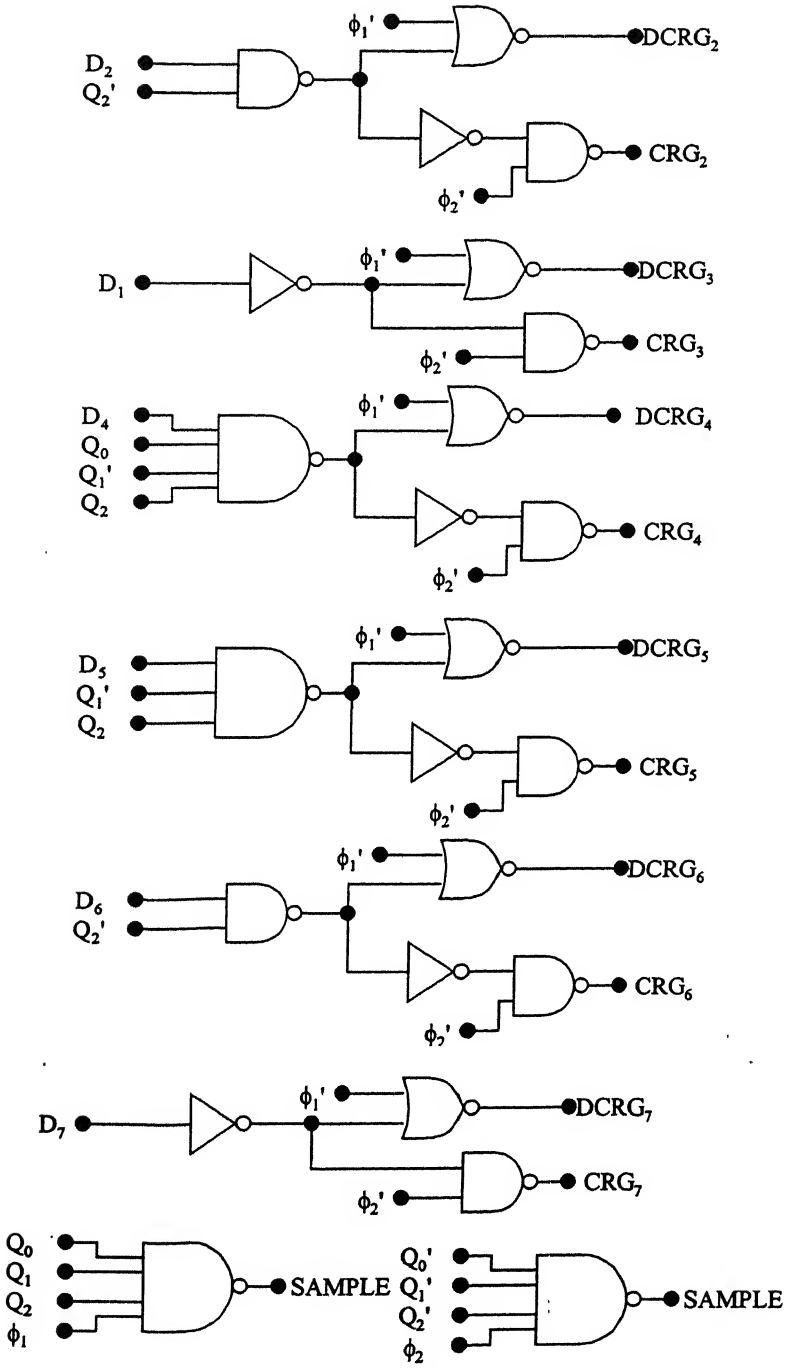


Figure D.3: Gate net-list of control and synchronization signal generator.

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